Semiconductor Device Theory:
MOSFETs–Theoretical Exercise

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1. Consider nearly two identical silicon MOSFETs. The only difference between the two devices is that the oxide layer in one of them is perfectly clean, and the other one is contaminated with sodium ions that produce a positive charge density. The concentration of sodium ions equals to $2\times10^{16} cm^{-3}$, and the thickness of the oxide layer is 0.1 μm. The permittivity of SiO_2 is $3.45\times10^{-11} F/m$.

   (a) What is the difference (including sign) in the device threshold voltages if these devices are *n*-channel devices?

   (b) What is the difference (including sign) in the device threshold voltages if these devices are *p*-channel devices?

   (c) Assume that the threshold voltage of the *n*-channel clean device is 1 V and that the threshold voltage of the *p*-channel clean device is -1 V. Sketch the qualitative dependencies of the drain-to-source saturation current on the gate voltage for all four devices (clean and contaminated *n*-channel and clean and contaminated *p*-channel devices). Label the thresholds and shifted thresholds on the gate-voltage axis.

2. Prove the expressions presented in the class for the extrinsic transconductance and the extrinsic drain conductance of a transistor with finite source and drain series resistances in terms of those of an ideal transistor with zero series resistances.

3. Calculate the dependence of the drain current I_D upon the drain voltage V_{DS} for V_{GS} = 5 V, for a silicon MOSFET with the following values of the source (R_S) and drain resistance (R_D): $R_S = R_D = 0\ \Omega$, and $R_S = R_D = 100\ \Omega$. The device parameters are as follows:

   gate length: L = 4 μm
   gate width: W = 100 μm
   electron mobility in the channel: $\mu_n = 1000\ cm^2/V\text{-}s$
   dielectric permittivity of gate oxide: $\varepsilon_{ox} = 3.45\times10^{-11}$ F/m
   dielectric permittivity of silicon: $\varepsilon_{sc} = 1.05\times10^{-10}$ F/m
   flat-band voltage: V_{FB} = 0 V
   substrate bias: V_{sub} = 0 V
   temperature: T = 300 K
   substrate doping: $N_A = 10^{15}\ cm^{-3}$
   gate oxide thickness: d_{ox} = 20 nm
   intrinsic carrier concentration: $n_i = 1.5\times10^{10}\ cm^{-3}$

   In your calculations use:
   (a) square-law theory
   (b) bulk-charge theory

Repeat the problem for $N_A=10^{16}$ cm^{-3} and $N_A=10^{17}$ cm^{-3}. Discuss the validity of the square-law theory versus substrate doping and the influence of the series resistance on the drain current characteristics of these devices.

4. Derive an expression for the drain saturation current of an *n*-channel MOSFET using square-law theory and neglecting velocity saturation effects, i.e. assuming the constant mobility model, but taking into account the source series resistance R_S. Use the following MOSFET parameters:

   gate oxide thickness: d_{ox} = 17.5 nm
   device gate width: W = 100 μm
   gate length: L = 4 μm
   threshold voltage: V_T = -1 V
   electron mobility in the channel: μ_n = 800 cm^2/V-s
   dielectric permittivity of gate oxide: $\varepsilon_{ox} = 3.45\times10^{-11}$ F/m
   gate voltage: V_{GS} = 5 V
   substrate bias: V_{sub} = 0 V

   Plot I_{Dsat} versus R_S for $2\Omega < R_S \leq 20\ \Omega$.

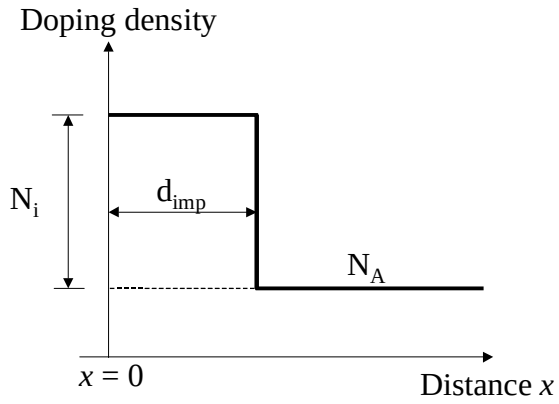
5. Calculate and plot the subthreshold current for a long-channel Si MOSFET as a function of the gate voltage V_{GS} that varies in the range between V_T - 1 (V) and V_T. For the drain voltage assume V_{DS} = 0.01 V, 0.1 V, and 10 V. Use the following parameters:

   threshold voltage: V_T = 1 V
   substrate doping: $N_A=10^{15}$ cm^{-3}
   electron mobility in the channel: : μ_n = 800 cm^2/V-s
   device gate width: W = 100 μm
   gate length: L = 20 μm
   gate oxide thickness: d_{ox} = 50 nm
   energy band gap: E_G = 1.12 eV
   effective density of states in the conduction band: $N_C = 3.22\times10^{19}$ cm^{-3}
   effective density of states in the valence band: $N_V = 1.83\times10^{19}$ cm^{-3}
   dielectric permittivity of gate oxide: $\varepsilon_{ox} = 3.45\times10^{-11}$ F/m
   dielectric permittivity of silicon: $\varepsilon_{sc} = 1.05\times10^{-10}$ F/m
   temperature: T = 300 K

6. Consider the following idealized ion implantation profile near the semiconductor-insulator interface in a Si MOSFET (x = 0 corresponds to the semiconductor insulator interface). Calculate the threshold voltage shift as a function of N_i, for 10^{14} cm$^{-3} \leq N_i \leq 10^{17}$ cm^{-3} for d_{imp} = 0.08 μm. Assume:

   semiconductor background doping $N_A = 10^{15}$ cm^{-3}
   gate oxide thickness: d_{ox} = 50 nm
   energy band gap: E_G = 1.12 eV
   effective density of states in the conduction band: $N_C = 3.22\times10^{19}$ cm^{-3}
   effective density of states in the valence band: $N_V = 1.83\times10^{19}$ cm^{-3}
   dielectric permittivity of gate oxide: $\varepsilon_{ox} = 3.45\times10^{-11}$ F/m
   dielectric permittivity of silicon: $\varepsilon_{sc} = 1.05\times10^{-10}$ F/m
   temperature: T = 300 K

   Assume shallow ionized acceptors. Define the threshold voltage as the gate voltage for which the electron concentration at the surface $n(0)$ is equal to $N_A + N_i$.



7. The current-voltage characteristics of a long-channel MOSFET are described with:

$$I_D = \begin{cases} \dfrac{Z\mu_{eff} C_{ox}}{L}\left[(V_G - V_T)V_D - \dfrac{1}{2}V_D^2\right], & V_D < V_G - V_T \\ \dfrac{Z\mu_{eff} C_{ox}}{2L}(V_G - V_T)^2, & V_D > V_G - V_T \end{cases}$$

where μ_{eff} is the effective electron mobility in the channel, L is the effective channel length, Z is the channel (gate) width, C_{ox} is the gate capacitance, I_D is the drain current, V_D is the drain voltage (with the source as reference), V_G is the gate voltage, and V_T is the threshold voltage. When the drain and gate are connected, consider the following two cases:

(a) $V_T > 0$, and

(b) $V_T < 0$.

Find and plot I_D in terms of V_D in each of these two cases.