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"Electronics from the Bottom Up: Physics of Nanoscale Transistors"

Exercises Comparing Ballistic MOSFETs to Real MOSFETs

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In "Physics of Nanoscale Transistors: Lecture 2: Elementary Theory of the Nanoscale MOSFET," we introduced a very simple theory of the ballistic MOSFET. The purpose of this exercise is to see how a ballistic MOSFET compares to an actual MOSFET. For the "actual" MOSFET, we will use the nano-CMOS simulation tool on nanoHUB.org. For the ballistic MOSFET, we will use the FETToy simulation tool on nanoHUB.org. (FETToy implements a more sophisticated version of the ballistic theory as described in Lectures 3 and 4 of "Physics of Nanoscale Transistors.")

To run a simulation tool, you will first have to apply for an account, which you can do with the Register link at the upper left of the nanoHUB main page. As soon as you have an account, you can proceed with the exercises below.

1) Use the simulation tool, nano-CMOS, to examine the IV characteristics of "45nm" N-channel CMOS technology. Select "NMOS 45nm," and use the default values. Push the Simulate button, and then extract the following key device metrics.

   a) The on-current in μA/μm
   b) The off-current in μA/μm
   c) The subthreshold swing, S, in mV/decade
   d) Estimate V_{DSAT} for V_{GS} = 1.0V.
   e) The DIBL in mV/V
   f) The threshold voltages, V_T(lin) and V_T(sat), in V
   g) The output resistance, R_o in Ω-μm
   h) The channel resistance, R_{ch} in Ω-μm
   i) The transconductance, g_m, in mS/mm at the maximum gate and drain voltage.

The FETToy simulation tool implements the ballistic MOSFET theory described in Lectures 3 and 4 of "Physics of Nanoscale Transistors," for ultra-thin-body (UTB) single and double gate MOSFETs. The 45nm CMOS device is a bulk MOSFET. Nevertheless, we will use FETToy for single gate, UTB ballistic MOSFETs to get a very rough idea of how the 45 nm NMOS transistor compares to the ballistic limit.

Note that FETToy contains an option, "Floating Boundary Flag." When turned on, this option allows the potential in the source to float, so that the ballistic source and drain can maintain charge neutrality under high gate and drain bias. For better results at high gate/drain biases, turn this flag on. For better results in the linear region (high gate, low drain bias) turn this flag off. In the spirit of our very rough comparison, we will turn this flag OFF for this for this exercise. Floating boundary conditions are discussed in Lecture 2, Part 2 and also in:

A. Rahman, J. Guo, S. Datta, and M. Lundstrom, "Theory of Ballistic Nanotransistors," IEEE Trans. Electron Dev., **50**, pp. 1853-1864, 2003.

Before running FETToy, you will need to specify several device input parameters. Some are physical parameters such as oxide thickness, power supply, and ambient temperature that you will need to select to be consistent with the nano-CMOS simulation. We also need to be sure that the two devices have similar subthreshoold swing and DIBL. Devices are usually compared for assuming that they have been designed to produce the same off-current.

The device-specific input parameters you need to specify to FETToy are:

a) gate insulator thickness: (set for consistency with nano-CMOS 45 nm)
b) gate insulator dielectric constant: (use 4.0)
c) threshold voltage: (set to produce the same off-current as nano-CMOS 45 nm)
d) gate control parameter, α_G: (set to produce same DIBL as nano-CMOS 45 nm)
e) drain control parameter, α_D: (set to produce the same DIBL as nano-CMOS 45 nm)
f) series resistance: (set to be the same as nano-CMOS 45 nm)

FETToy uses a gate control parameter, α_G, to set the subthreshold swing according to:

$$\alpha_G = \frac{C_G}{C_\Sigma} = \frac{2.3k_BT}{q} \times \frac{1}{S}$$

and it uses a drain control parameter, α_D, to set the DIBL according to:

$$\alpha_D = \frac{C_D}{C_\Sigma} = \frac{2.3k_BT}{q} \times \frac{DIBL}{S}$$

where

C_Σ = total capacitance = $C_G + C_D + C_S$

S = subthreshold swing

DIBL = Drain Induced Barrier Lowering

2) List the FETToy device input parameters you used, then run a FETToy simulation. (You may need to iterate a few times to get the correct input parameters like threshold voltage.) Then extract the same device metrics as those listed in question 1).

3) Compare the “actual” 45 nm NMOS transistor from nano-CMOS to its ballistic counterpart from FETToy. (Note that the FETToy is not really ballistic because a series resistance is included. Compare the channel resistances (you will need to subtract out the series resistance) and the on-currents of the two devices. To what extent can a modern N-MOSFET be considered to be an intrinsic ballistic transistor with two series resistances attached to the source and drain contacts?