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"Electronics from the Bottom Up"

Exercises on Ballistic MOSFET Theory

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Objective:
The objective of these exercises is to help you gain familiarity with the theory of the ballistic MOSFET as presented in "Physics of Nanoscale Transistors: Lecture 3: Theory of the Ballistic MOSFET."

1) The location of the Fermi level with respect to the bottom of the subband, η_{F1}, is a key parameter in the theory.

   a) Show that for high drain bias, η_{F1} is obtained from

$$\eta_{F1} = \ln\left[\exp\left(\frac{2n_S(0)}{qN_{2D}}\right) - 1\right].$$

   Clearly identify the assumptions you make.

   b) Using the expression above and numbers appropriate for (100) silicon, compute $\left(E_F - \varepsilon_1(0)\right)$ when $n_S(0) = 10^{13}$ cm^{-2}. You should assume (100) silicon with a single (unprimed) subband occupied.

   c) Derive an analogous expression for low drain voltage.

2) Use the results of question 1) to show that the drain saturation voltage for a ballistic MOSFET is

$$V_{DSAT} = \left(k_B T/q\right)\ln\left[\exp\left(\frac{2C_{OX}\left(V_{GS} - V_T\right)}{qN_{2D}}\right) - 1\right]$$

3) Show that for strong carrier degeneracy, the injection velocity approaches

$$\tilde{\upsilon}_T \rightarrow \upsilon_T \frac{4}{3\sqrt{\pi}} \eta_{F1}^{1/2}$$

HINT: Refer to "Notes on Fermi Dirac Integrals, 2nd Ed." by Raseong Kim and Mark Lundstrom.

4) Use the results of question 3) to show that for strong carrier degeneracy, $\upsilon_T \sim \left(V_{GS} - V_T\right)^{1/2}$ and that $I_D \sim \left(V_{GS} - V_T\right)^{3/2}$.

5) The Fermi velocity is given by $\upsilon_F = \hbar k_F / m^*$. Show that for strong carrier degeneracy, $\tilde{\upsilon}_T \rightarrow \left(4/3\pi\right)\upsilon_F$.

HINT: Refer to "Notes on Fermi Dirac Integrals, 2nd Ed." by Raseong Kim and Mark Lundstrom.

6) In Lecture 3, we showed a plot of ballistic injection velocity, $\tilde{\upsilon}_T$ vs. inversion layer density, $n_S(0)$. Reproduce this plot and compare the injection velocity vs. $n_S(0)$ for Si ($m^*/m_0 = 0.19$) to that for $In_{0.7}Ga_{0.3}As$ ($m^*/m_0 = 0.037$). The results should help you understand why device researchers are currently exploring III-V channel MOSFETs.

7) In Lecture 3, we showed that the saturated drain current varies with V_{GS} according to $I_D \propto \left(V_{GS} - V_T\right)^{\alpha}$ where $\alpha = 1$ in the non-degenerate case and $\alpha = 1.5$ in the degenerate case. What happens in the typical case for modern transistors? Assume $V_{DD} = 1.0$V, $t_{ox} = 1.2$ nm, $V_T = 0.3$V, and compute I_D vs. V_{GS} for $V_{DD} = 1.0$V and determine the parameter, α. (Note that t_{ox} is actually an effective, electrical, thickness that accounts for the influence of the semiconductor capacitance and the depletion of the poly silicon gate. Using this effective thickness in the conventional expression, $C_{ox} = \kappa_{ox}\varepsilon_0 / t_{ox}$, produces a reasonable estimate for the oxide capacitance. Assume that $\kappa_{ox} = 4$.)

8) In Lecture 3, we obtained an expression for the ballistic channel conductance as

$$G_{CH} = \frac{1}{R_{CH}} = \left(WC_{ox}\left(V_{GS} - V_T\right)\frac{\upsilon_T}{\left(2k_BT/q\right)} \right)\left[\frac{\mathcal{F}_{-1/2}\left(\eta_{F1}\right)}{\mathcal{F}_0\left(\eta_{F1}\right)} \right]$$

where R_{CH} is the channel resistance. Compute the ballistic channel resistance for a modern transistor with the following parameters.

V_{DD} = 1.0V
t_{ox} = 1.2 nm
V_T = 0.3V

(Note that t_{ox} is actually an effective, electrical, thickness that accounts for the influence of the semiconductor capacitance and the depletion of the poly silicon gate. Using this effective thickness in the conventional expression, $C_{ox} = \kappa_{ox}\varepsilon_0 / t_{ox}$, produces a reasonable estimate for the oxide capacitance. Assume that $\kappa_{ox} = 4$.)

a) Compute the result and express your answer in the units of Ω-micrometers .

b) Compare your answer to the typical value of the series resistance, $R_S = R_D = 100$ Ω-micrometer .

c) Compare your answer to the conventional expression for the channel resistance of a MOSFET,

$$G_{CH} = \frac{1}{R_{CH}} = \frac{W}{L}\mu_{eff} C_{ox}\left(V_{GS} - V_T\right),$$

assuming an effective mobility for electrons of $\mu_{eff} = 200$ cm^2/V-s and a channel length of 50 nm.

d) In general, we can define, $G_{CH} \equiv M\, 2q^2/h$. For T = 0K, M is an integer number of conducting channels, but more generally, we can use this expression to estimate the effective number of channels. Use your answer for part a) to determine how many channels are conducting for a W = 1 μm wide MOSFET and for a minimum width MOSFET with W = 100nm.

e) As discussed in Lesson 2, we can define a "ballistic mobility" as

$$\mu_B = \frac{\upsilon_T L}{\left(2k_B T/q\right)}\left[\frac{\mathcal{F}_{-1/2}\left(\eta_{F1}\right)}{\mathcal{F}_0\left(\eta_{F1}\right)}\right],$$

which is the highest value of mobility that one could deduce from the linear region of the I-V characteristic. Assume L = 50nm and compute the ballistic mobility for this MOSFET and compare it to the real mobility of $\mu_{eff} = 200$ cm^2/V-s .

9) Begin with the general current expression,

$$I_D = WC_{ox}\left(V_{GS} - V_T\right)\tilde{\upsilon}_T\left[\frac{1 - \mathcal{F}_{1/2}\left(\eta_{F2}\right)/\mathcal{F}_{1/2}\left(\eta_{F1}\right)}{1 + \mathcal{F}_0\left(\eta_{F2}\right)/\mathcal{F}_0\left(\eta_{F1}\right)}\right]$$

and show that the ballistic channel conductance is

$$G_{CH} = \left(WC_{ox}\left(V_{GS} - V_T\right)\frac{\upsilon_T}{\left(2k_BT/q\right)}\right)\left[\frac{\mathcal{F}_{-1/2}\left(\eta_{F1}\right)}{\mathcal{F}_0\left(\eta_{F1}\right)}\right].$$

10) In the $T = 0$ limit, we expect $G_{CH} = M\,2q^2/h$. It is hard to take this limit from our final expression for the channel conductance,

$$G_{CH} = \frac{1}{R_{CH}} = \left(WC_{ox}\left(V_{GS} - V_T\right)\frac{\upsilon_T}{\left(2k_BT/q\right)}\right)\left[\frac{\mathcal{F}_{-1/2}\left(\eta_{F1}\right)}{\mathcal{F}_0\left(\eta_{F1}\right)}\right].$$

It is easier to evaluate $I^+\left(\eta_{F1}\right)$ and $I^+\left(\eta_{F1}\right)$ in the $T = 0$K limit and then deduce the ballistic conductance from those expressions. Use either approach and show that $G_{CH} = M\,2q^2/h$ for $T = 0$K.

11) The on-current of a modern MOSFET is about 1.0 mA/mm. In lesson 2, we derived an expression for the on-current of a ballistic MOSFET as

$$I_D \to WC_{ox}\left(V_{DD} - V_T\right)\tilde{\upsilon}_T .$$

Compute the ballistic on-current for a modern transistor with the following parameters.

$V_{DD} = 1.0$V
$t_{ox} = 1.2$ nm
$V_T = 0.3$V

(Note that t_{ox} is actually an effective, electrical, thickness that accounts for the influence of the semiconductor capacitance and the depletion of the poly silicon gate. Using this effective thickness in the conventional expression, $C_{ox} = \kappa_{ox}\varepsilon_0/t_{ox}$, produces a reasonable estimate for the oxide capacitance. Assume that $\kappa_{ox} = 4$.)

What fraction of the ballistic limit does the actual device deliver?

12) In Lecture 3, we derived an expression for the drain saturation voltage,

$$V_{DSAT} \approx (k_B T/q)\eta_{F1} = (k_B T/q)\ln\left[\exp\left(\frac{2C_{OX}(V_{GS}-V_T)}{qN_{2D}}\right)-1\right].$$

Compute V_{DSAT} vs. $V_{GS} - V_T$ for a transistor with the following parameters.

V_{DD} = 1.0V
t_{ox} = 1.2 nm
V_T = 0.3V

(Note that t_{ox} is actually an effective, electrical, thickness that accounts for the influence of the semiconductor capacitance and the depletion of the poly silicon gate. Using this effective thickness in the conventional expression, $C_{ox} = \kappa_{ox}\varepsilon_0/t_{ox}$, produces a reasonable estimate for the oxide capacitance. Assume that $\kappa_{ox} = 4$.)

If we can ignore the -1 in the expression for V_{DSAT}, then

$$V_{DSAT} = \frac{(2k_B T/q)C_{ox}}{qN_{2D}}(V_{GS}-V_T) = \beta(V_{GS}-V_T).$$

Compute β for this transistor and plot the approximate expression on the same graph as the correct expression. Note that V_{DSAT} for a ballistic MOSFET is the long channel V_{DSAT}, $V_{DSAT} = (V_{GS} - V_T)$ multiplied by a parameter that is less than one.

13) The I-V characteristic of a ballistic MOSFET is given by:

$$I_{DS} = WC_{ox}(V_{GS}-V_T)\tilde{\upsilon}_T\left[\frac{1-\mathcal{F}_{1/2}(\eta_{F2})/\mathcal{F}_{1/2}(\eta_{F1})}{1+\mathcal{F}_0(\eta_{F2})/\mathcal{F}_0(\eta_{F1})}\right]$$

$$\tilde{\upsilon}_T \equiv \sqrt{\frac{2k_B T}{\pi m^*}}\frac{\mathcal{F}_{1/2}(\eta_{F1})}{\mathcal{F}_0(\eta_{F1})} = \upsilon_T\frac{\mathcal{F}_{1/2}(\eta_{F1})}{\mathcal{F}_0(\eta_{F1})}$$

$$C_{OX}(V_{GS}-V_T) = q\frac{N_{2D}}{2}\left[\mathcal{F}_0(\eta_{F1})+\mathcal{F}_0(\eta_{F2})\right]$$

$$\eta_{F2} = \eta_{F1} - qV_{DS}/k_B T$$

Using these equations, write a Matlab script to compute I_D vs. V_{DS} for V_{GS} = 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, and 1.0V. Assume a transistor described by:

V_{DD} = 1.0V
t_{ox} = 1.2 nm
V_T = 0.3V

(Note that t_{ox} is actually an effective, electrical, thickness that accounts for the influence of the semiconductor capacitance and the depletion of the poly silicon gate. Using this effective thickness in the conventional expression, $C_{ox} = \kappa_{ox}\varepsilon_0 / t_{ox}$, produces a reasonable estimate for the oxide capacitance. Assume that $\kappa_{ox} = 4$.)