A Broad Overview of Reliability of Semiconductor MOSFET

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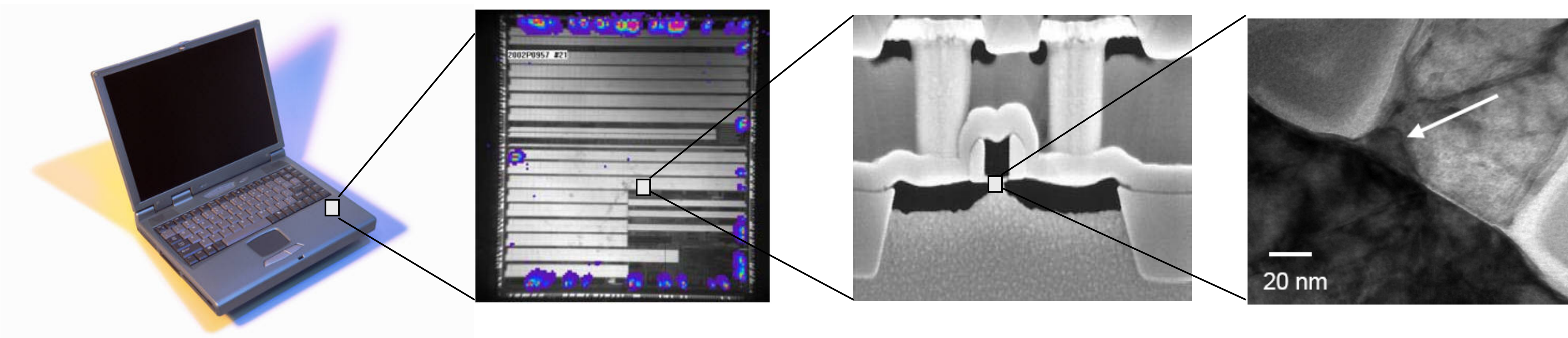
Warranty, product recall and other facts of life …

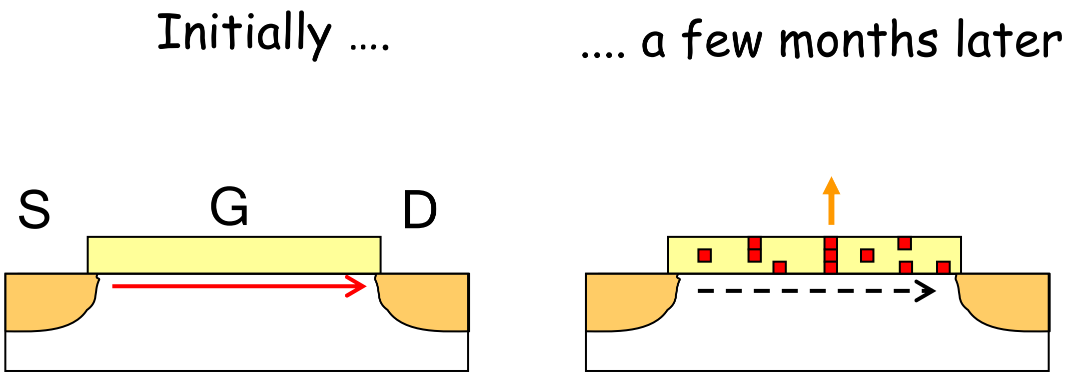


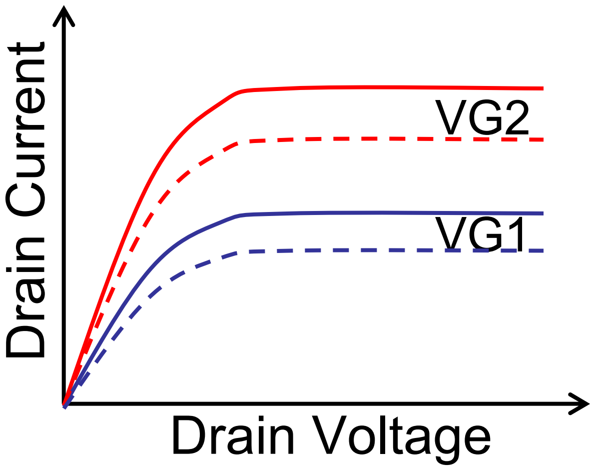
In this course, you are learning how to design MOSFETs that go in an IC …

… because the ICs operate in incredibly harsh conditions, turning on and off trillions of time during its lifetime ….

… therefore the properties of the MOSFET keep changing. Eventually, S/D can be shorted, the gate oxide can break, etc ….

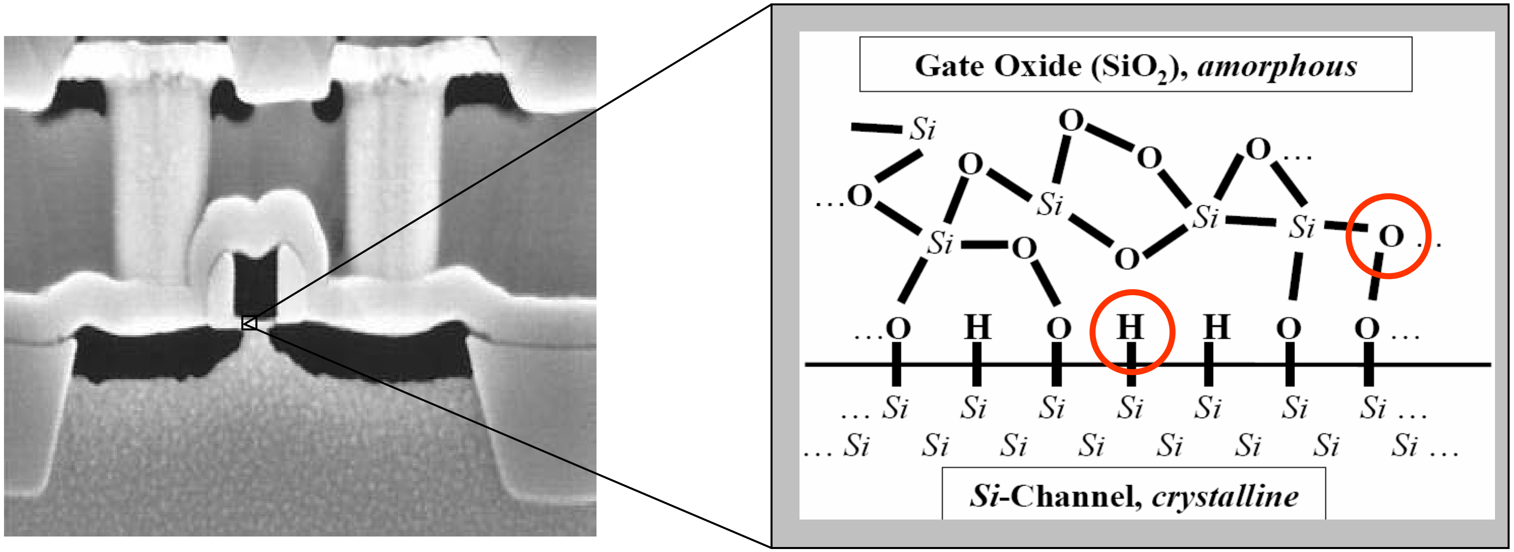
Transistor Reliability Issues





- Negative Bias Temperature Instability (NBTI)
- Hot carrier degradation (HCI)
- Gate dielectric Breakdown (TDDB)
- Electrostatic Discharge (ESD)
- Radiation Damage, Single Event Upset, Latch-up

Si-H and Si-O broken bonds



Broken Si-H bonds

Negative Bias Temperature Instability (NBTI)

Hot carrier degradation (HCI)

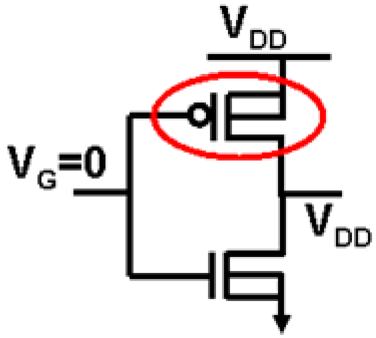
Broken Si-O bonds

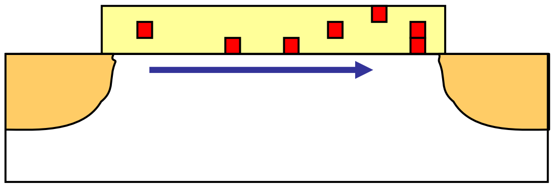
Gate dielectric Breakdown (TDDB)

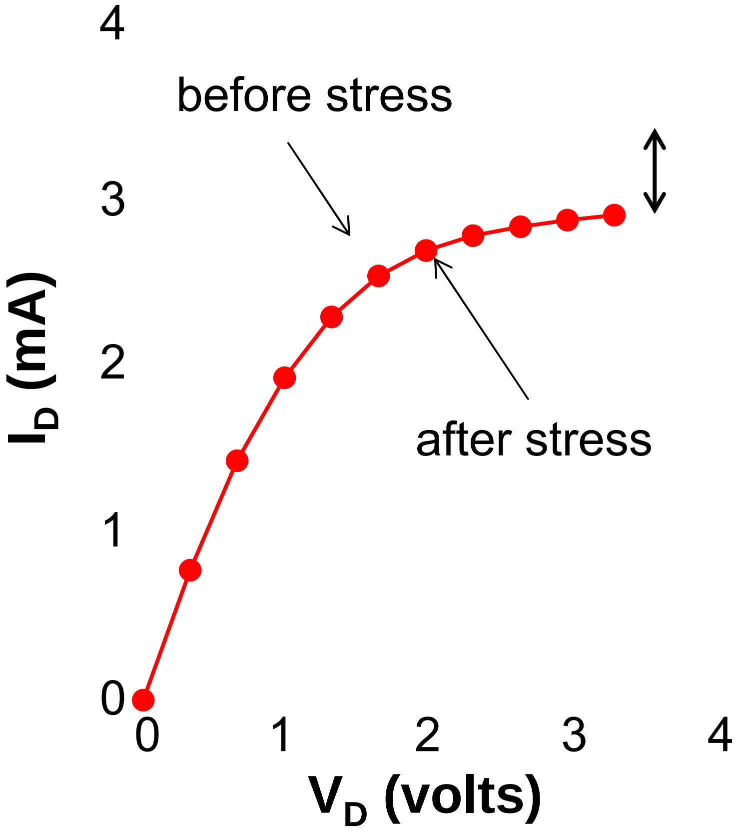
Electrostatic Discharge (ESD)

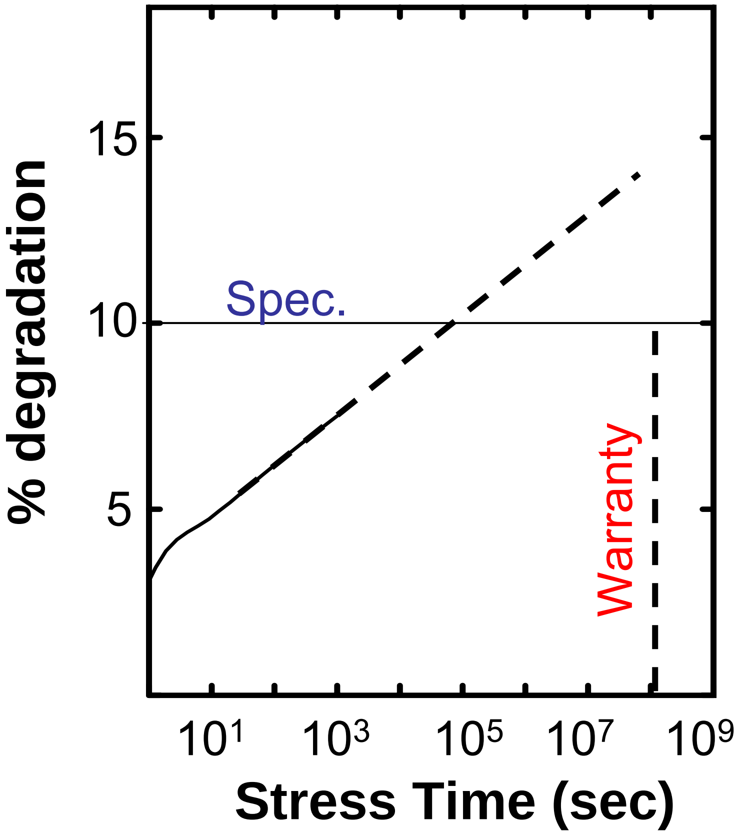
Radiation induced Gate Rupture (RBD)

NBTI Defined …



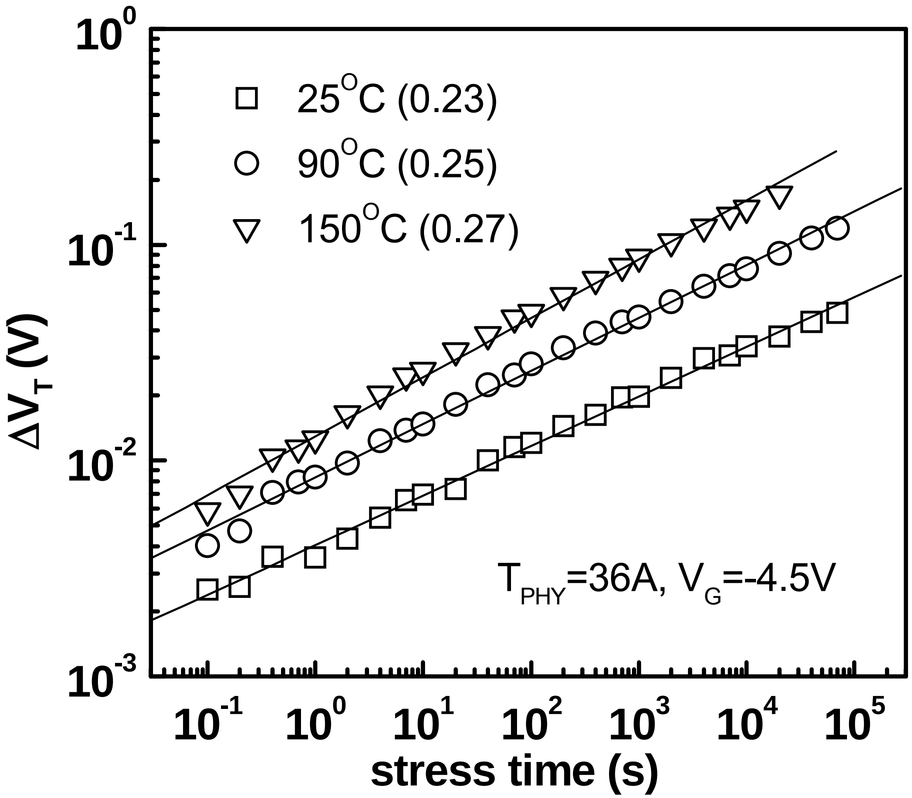






Characteristics of NBTI Degradation ...

$$\Delta V_T = A e^{-Ea/k_B T} t^n$$



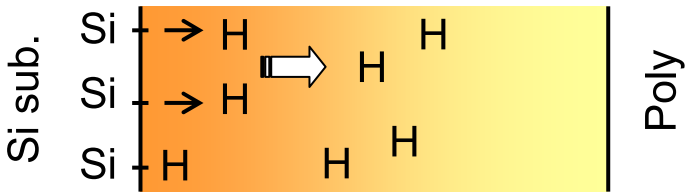
- n ~ 0.25
- Ea ~ 0.5 eV
- A depends on Eox

Where does this very strange characteristics come from?

Lecture: www.nanohub.org/resources/193

Simulator: www.nanohub.org/resources/1647

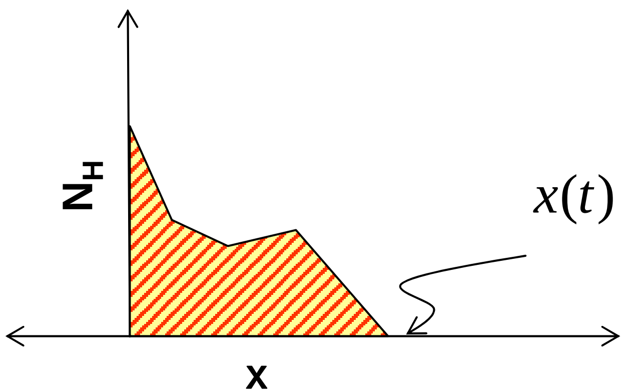
The R-D Model and its reformulation



$$\frac{dN_{IT}}{dt} = k_F(N_0 - N_{IT}) - k_R N_H(0) N_{IT}$$

If trap generation is small, & $N_{IT} < N_0$,

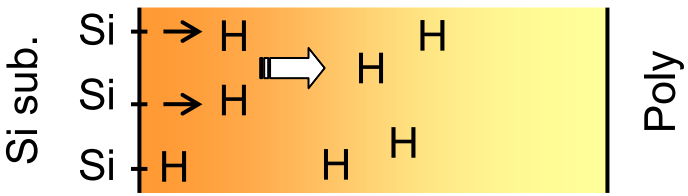
$$\left(\frac{k_F N_0}{k_R}\right) \approx N_H(0) N_{IT}$$

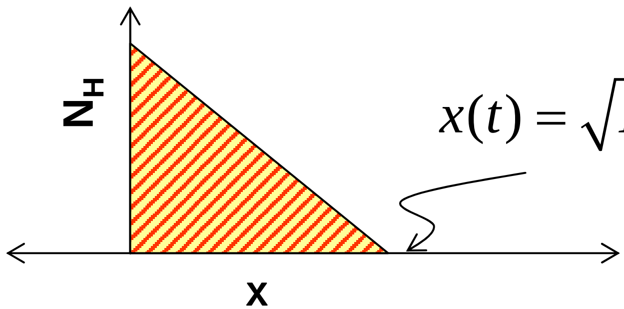


$$\frac{dN_{IT}}{dt} = D_H \frac{d^2 N_H}{dx^2} + N_H \mu_H E + \frac{\delta}{2}\frac{dN_H}{dt}$$

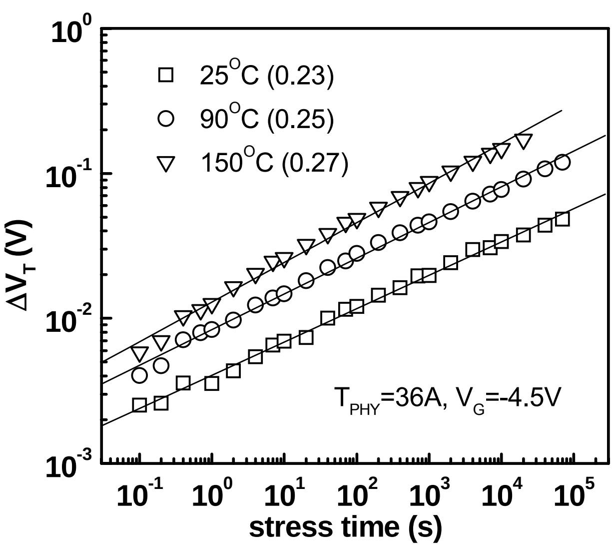
$$N_{IT}(t) = \int_{x=0}^{x(t)=f(D_H,\mu_H,t)} N_H(x,t)\,dx$$

N_{IT} with *Neutral* H Diffusion





$$x(t) = \sqrt{D_H t}$$



$$\left(\frac{k_F N_0}{k_R}\right) \approx N_H(0) N_{IT}$$

$$N_{IT}(t) = \int_0^{\sqrt{D_H t}} N_H(x,t)\,dx$$

$$= \frac{1}{2} N_H(0) \sqrt{D_H t}$$

Combining these two, we get

$$N_{IT}(t) = \sqrt{\frac{k_F N_0}{2k_R}}(D_H t)^{1/4}$$

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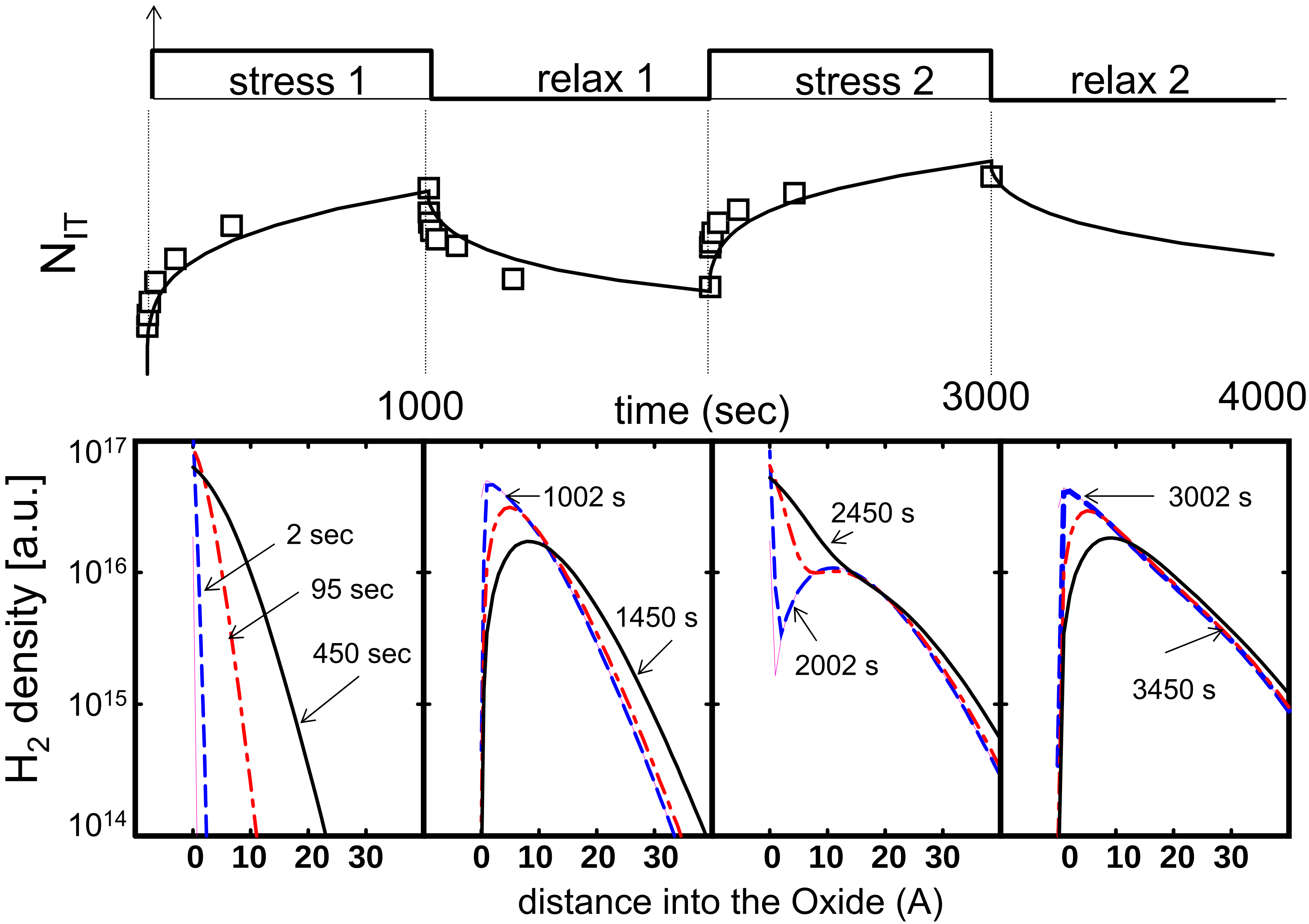
n=1/4 even with two sided diffusion

n ~ 1/4 is a possible signature of neutral H diffusion

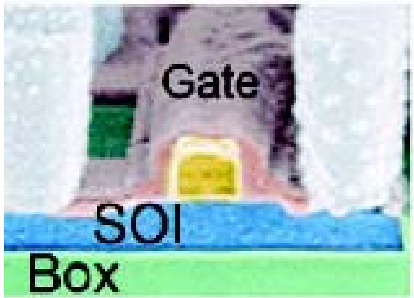
Reproduces results of Jeppson, JAP, 1977.

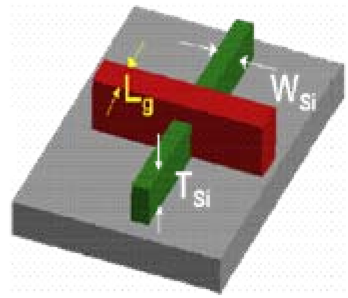
R-D Model at Low Frequencies

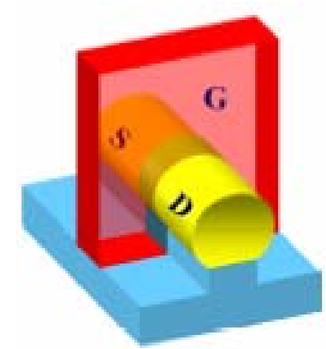


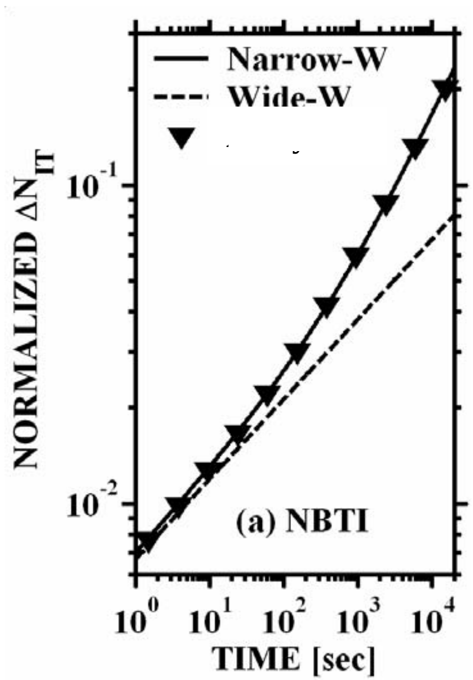
Alam, IEDM 2003

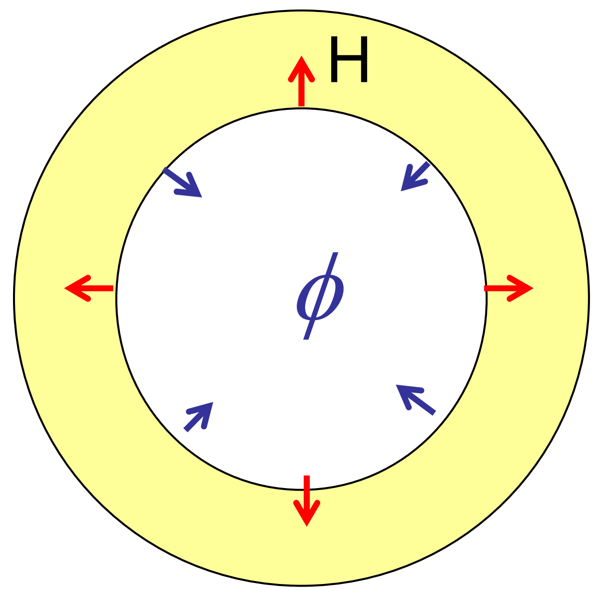
Future of Non-planar Transistors









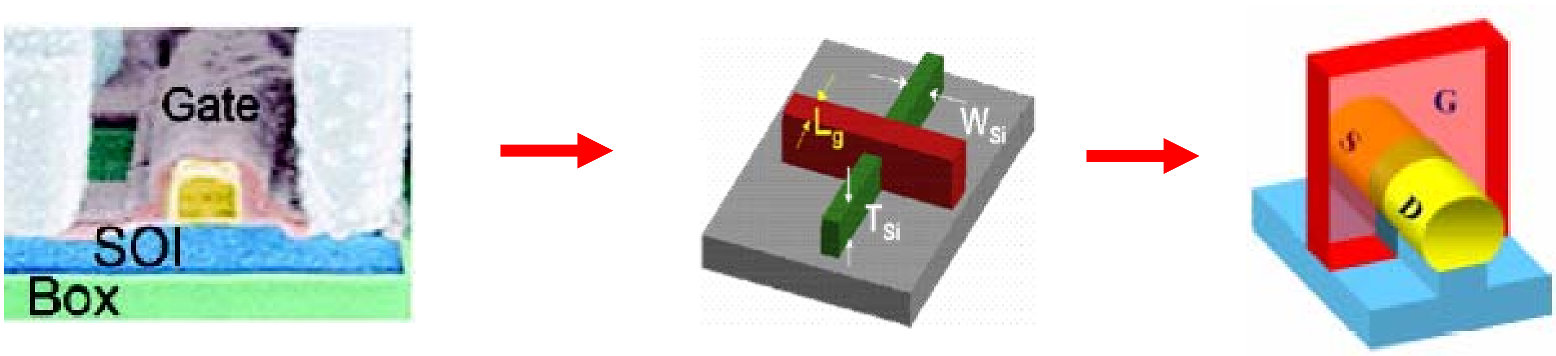


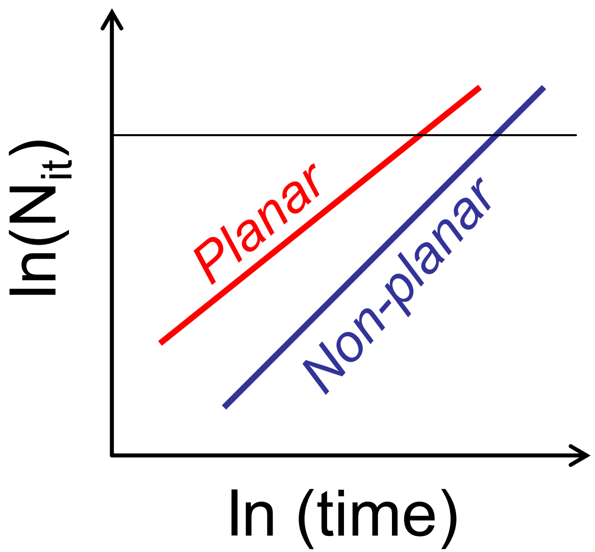
$$\varepsilon \nabla^2 \phi = 0$$

$$D_H \nabla^2 N_H = 0$$

Reliability theory can predict performance-degradation trade-off.

Performance and Reliability



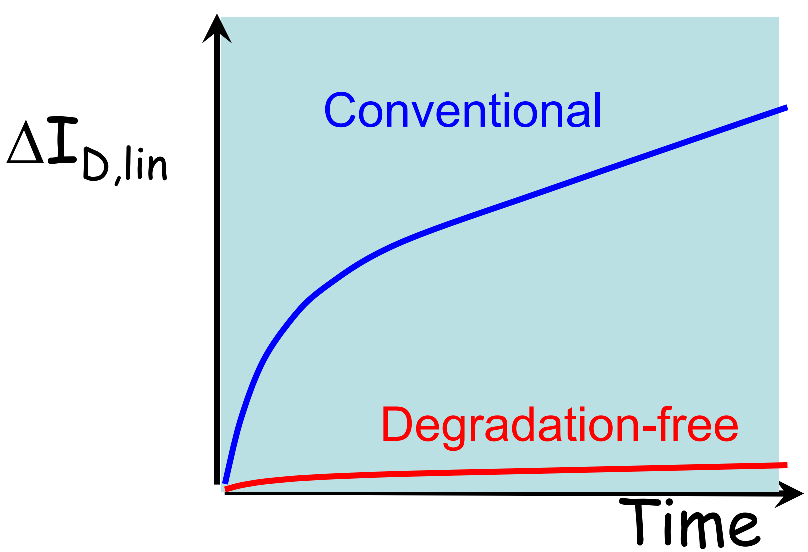


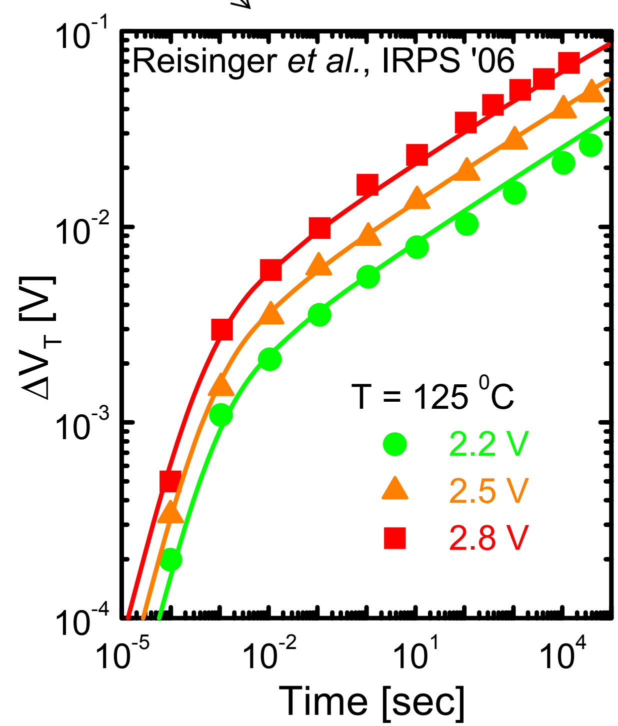
H. Kufluoglu, TED, 2006

Could strained transistors degradation-free?

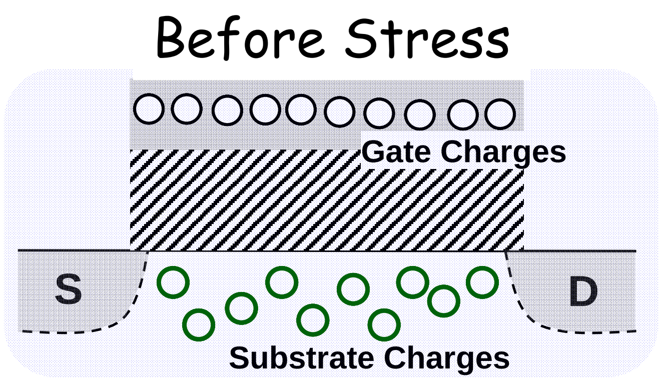
$$-\frac{\Delta I_D}{I_{D0}} = \frac{\Delta \mu_{eff}}{\mu_{eff0}} - \frac{\Delta V_T}{V_G - V_{T0}} \qquad I_D = A\,\mu_{eff}\left(V_G - V_T\right)$$

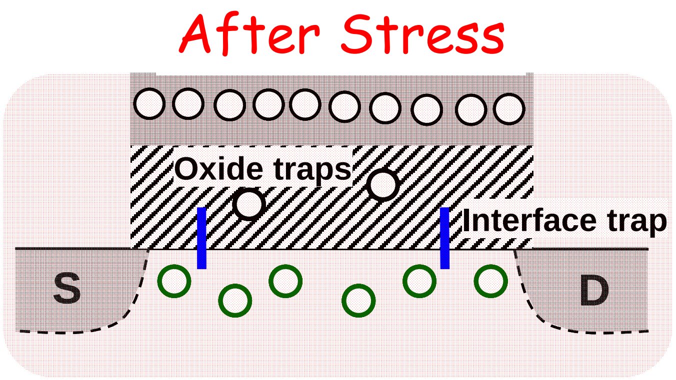
If we could make $\Delta\mu$ positive ...



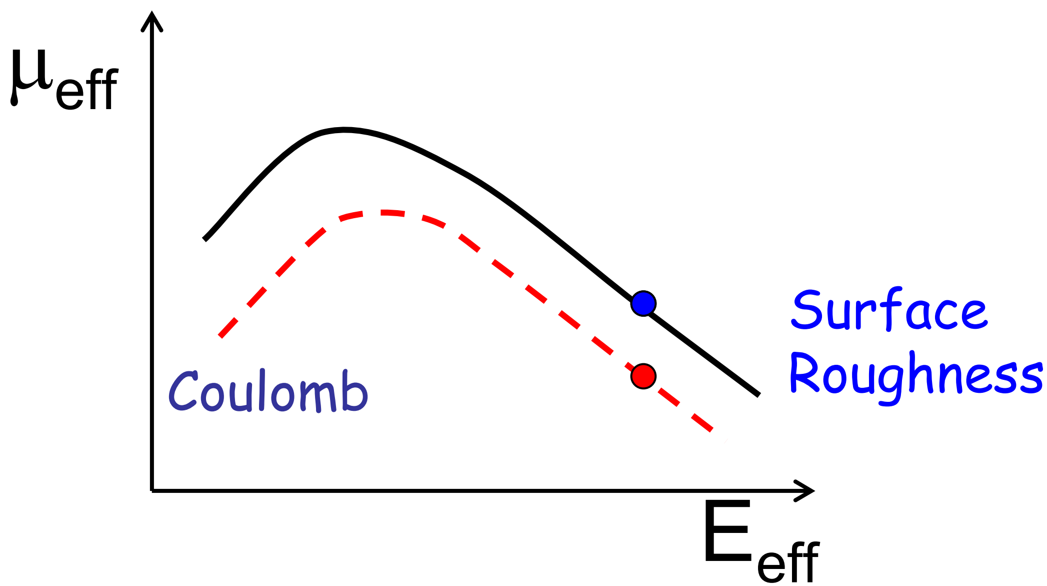


Threshold voltage and Effective Field …



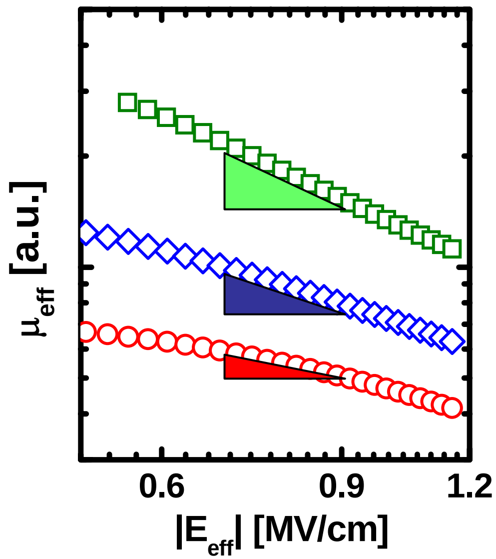


$$E_{eff} = Q_{dep} + \eta Q_{inv} \sim (V_G - V_T)$$

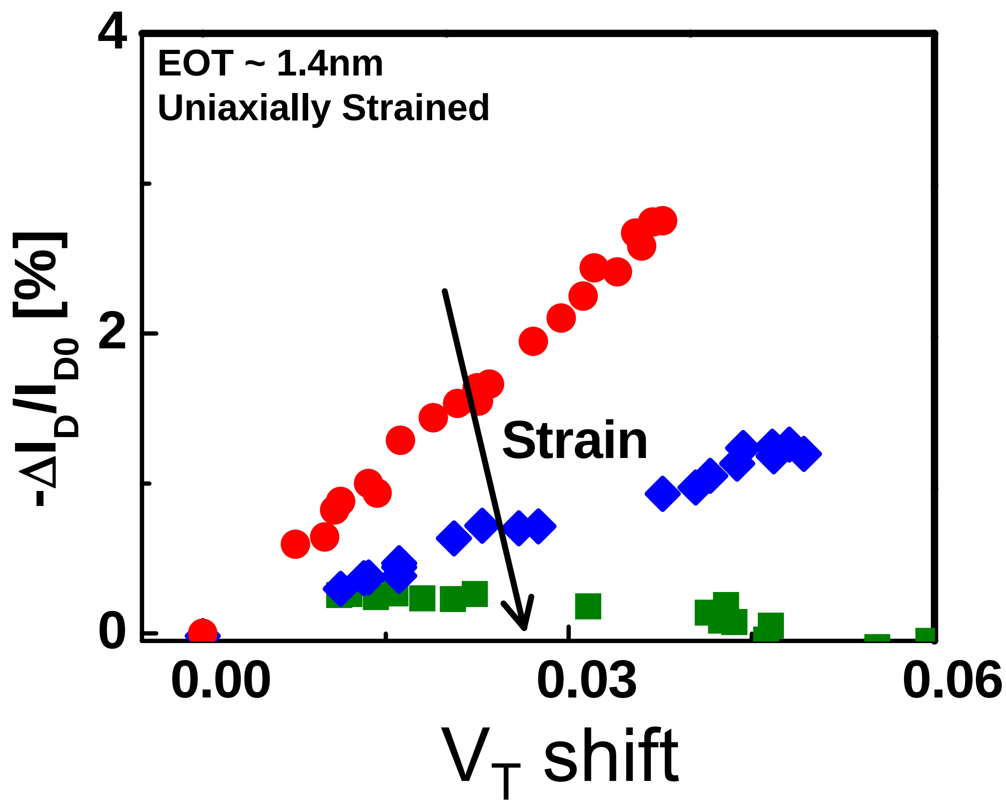


Degradation-free logic transistors …

$$-\frac{\Delta I_D}{I_{D0}} = \frac{\Delta \mu_{eff}}{\mu_{eff0}} - \frac{\Delta V_T}{V_G - V_{T0}}$$

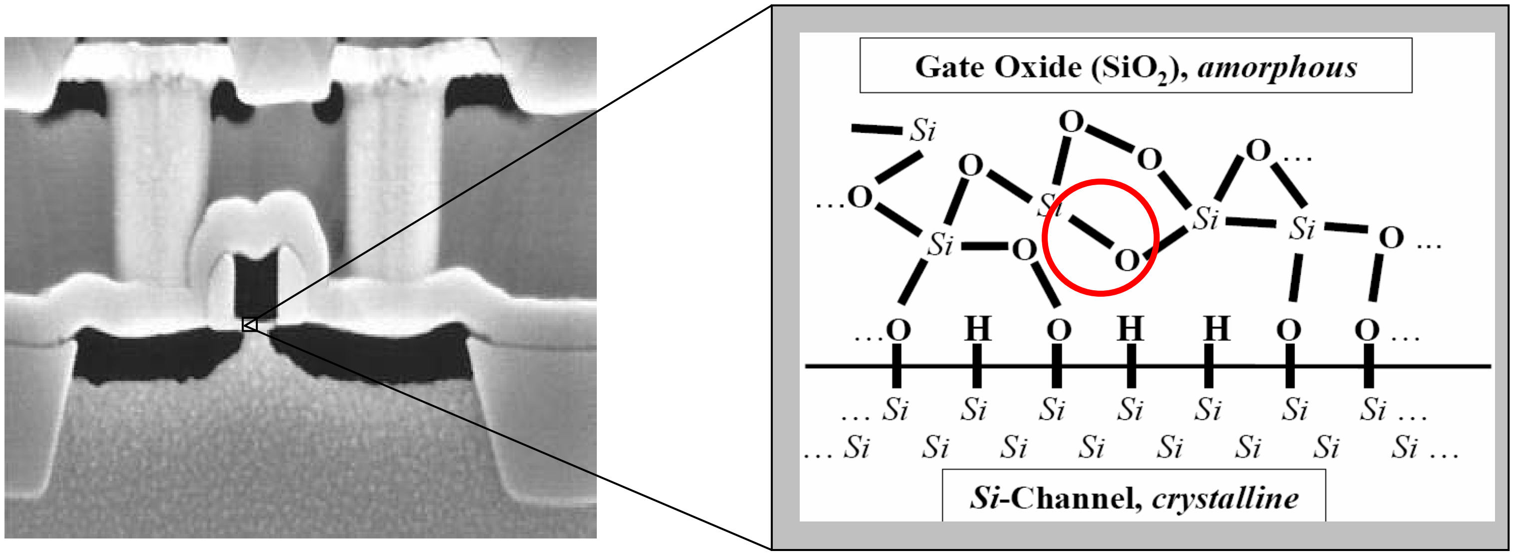


By strain engineering



E. Islam, APL, 2008

Outline: Si-H and Si-O Bonds



Broken Si-H bonds

Negative Bias Temperature Instability (NBTI)

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Broken Si-O bonds

Gate dielectric Breakdown (TDDB)

Electrostatic Discharge (ESD)

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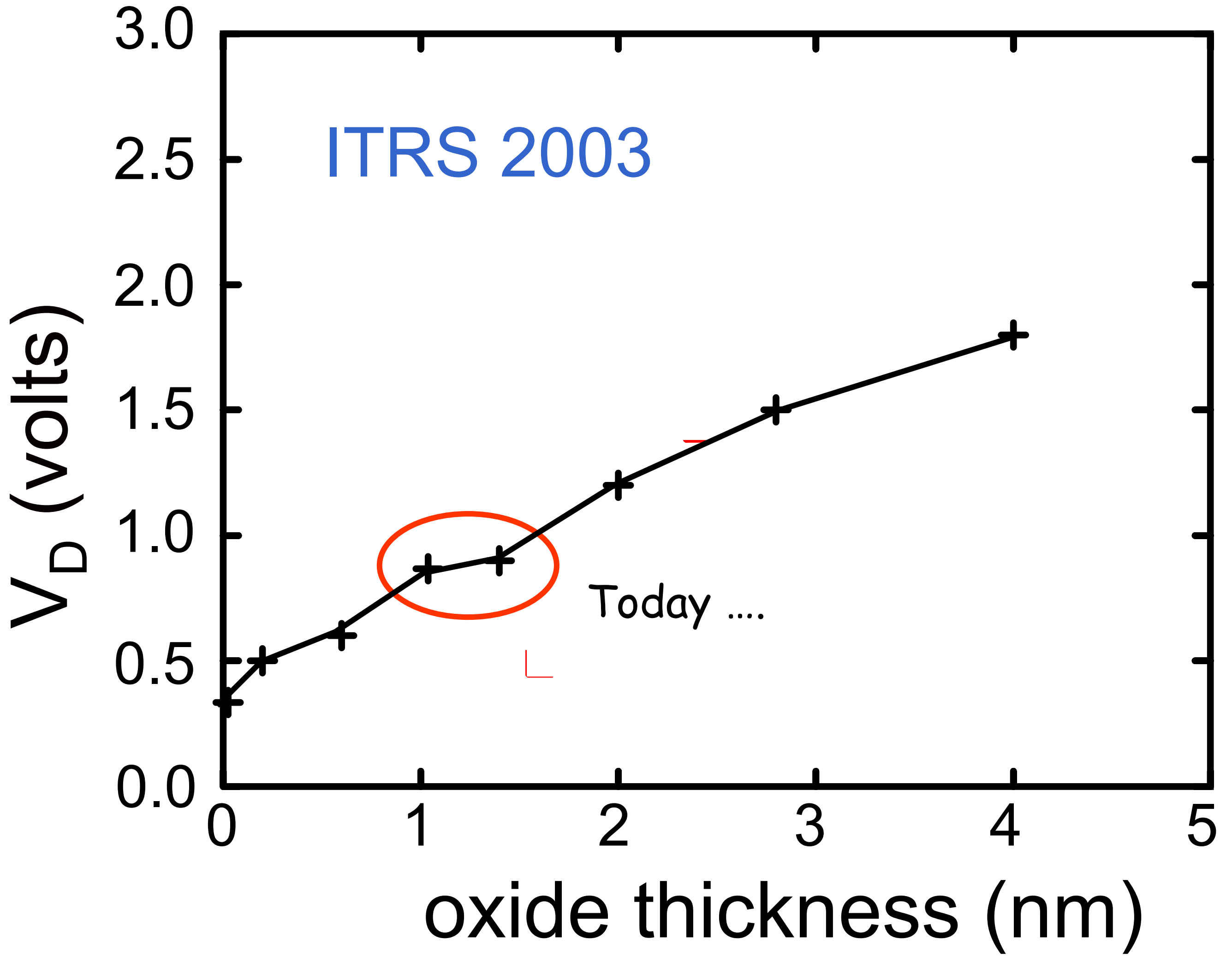
Oxide Thickness and Supply Voltage Scaling

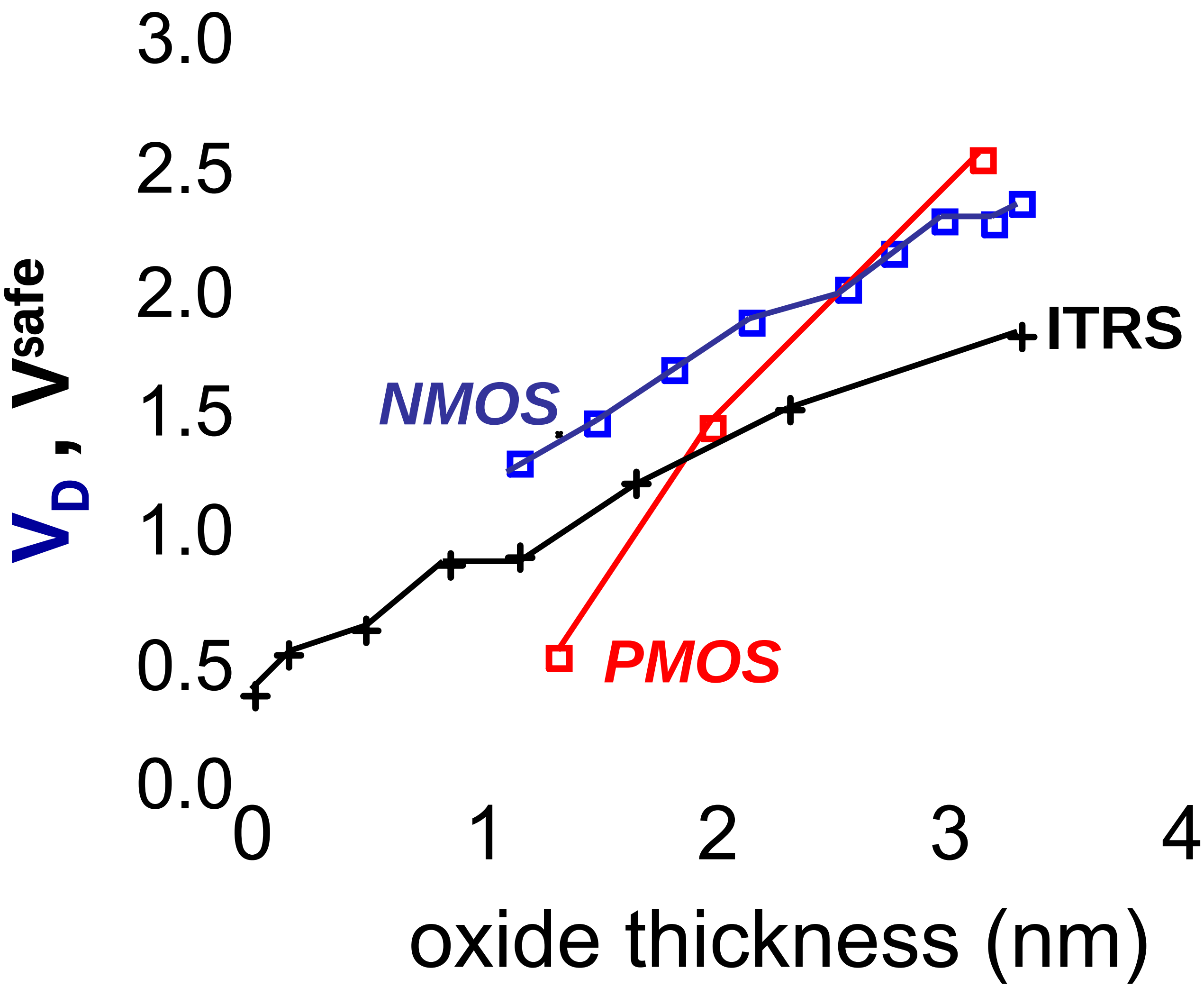


Power/Speed

⇧ $I_D = k\left(V_D - V_T\right)\frac{\upsilon}{T_{ox}}$

⇩ $P = CV_D^2 f$

Gate Dielectric Breakdown in NMOS and PMOSFETs



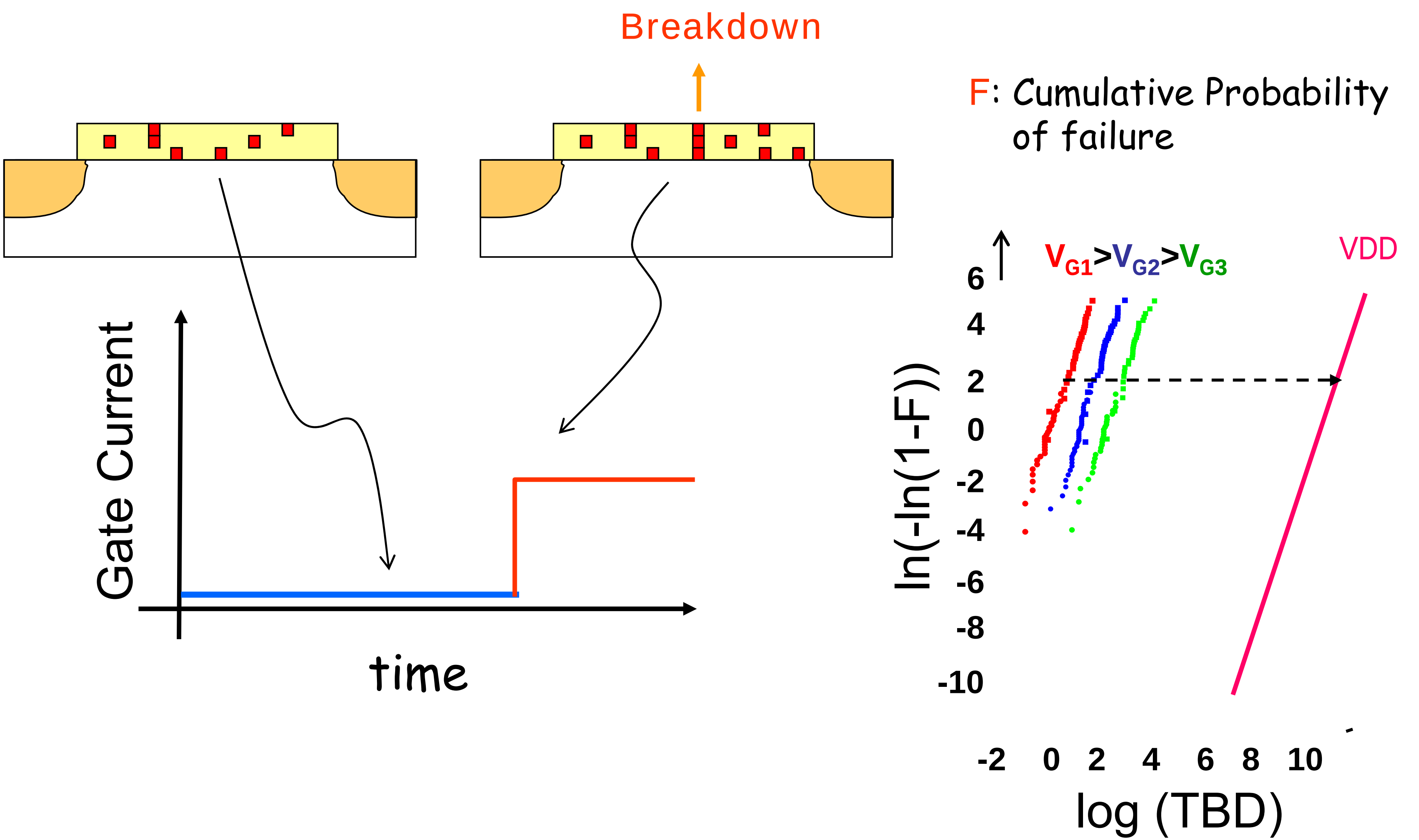
V_{safe} can be calculated

Historically NMOS TDD limited oxide scaling

Below 3 nm, PMOS TD defines scaling limit

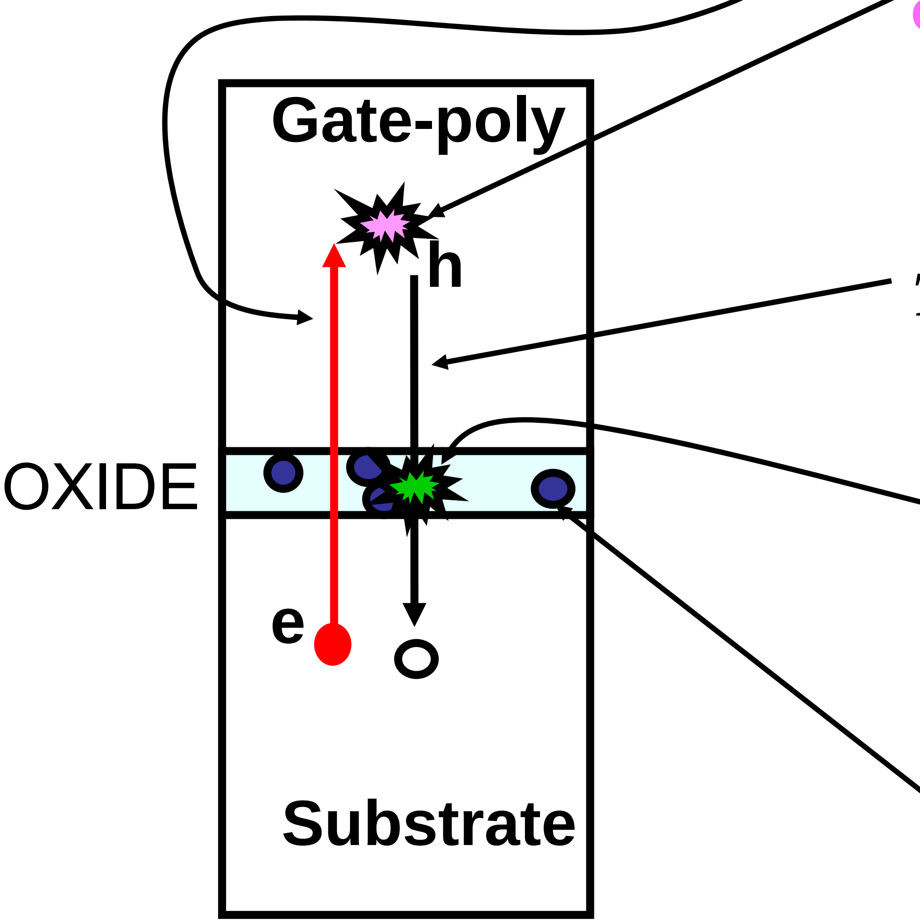
SBD allows adequate reliability even < 3nm.

Stages of Gate Dielectric Breakdown



Theory of Anode Hole Injection

$$T_{BD} = \left(\frac{N_{BD}}{k}\right)^n \frac{1}{J_e \alpha T_p}$$



J_e - Electron current density

α - Impact Ionization Rate

(probability that a hole will be created by an incoming electron)

T_p - **Transmission Rate**

(probability that the hole will travel through the oxide layer)

k - Trap Generation Efficiency

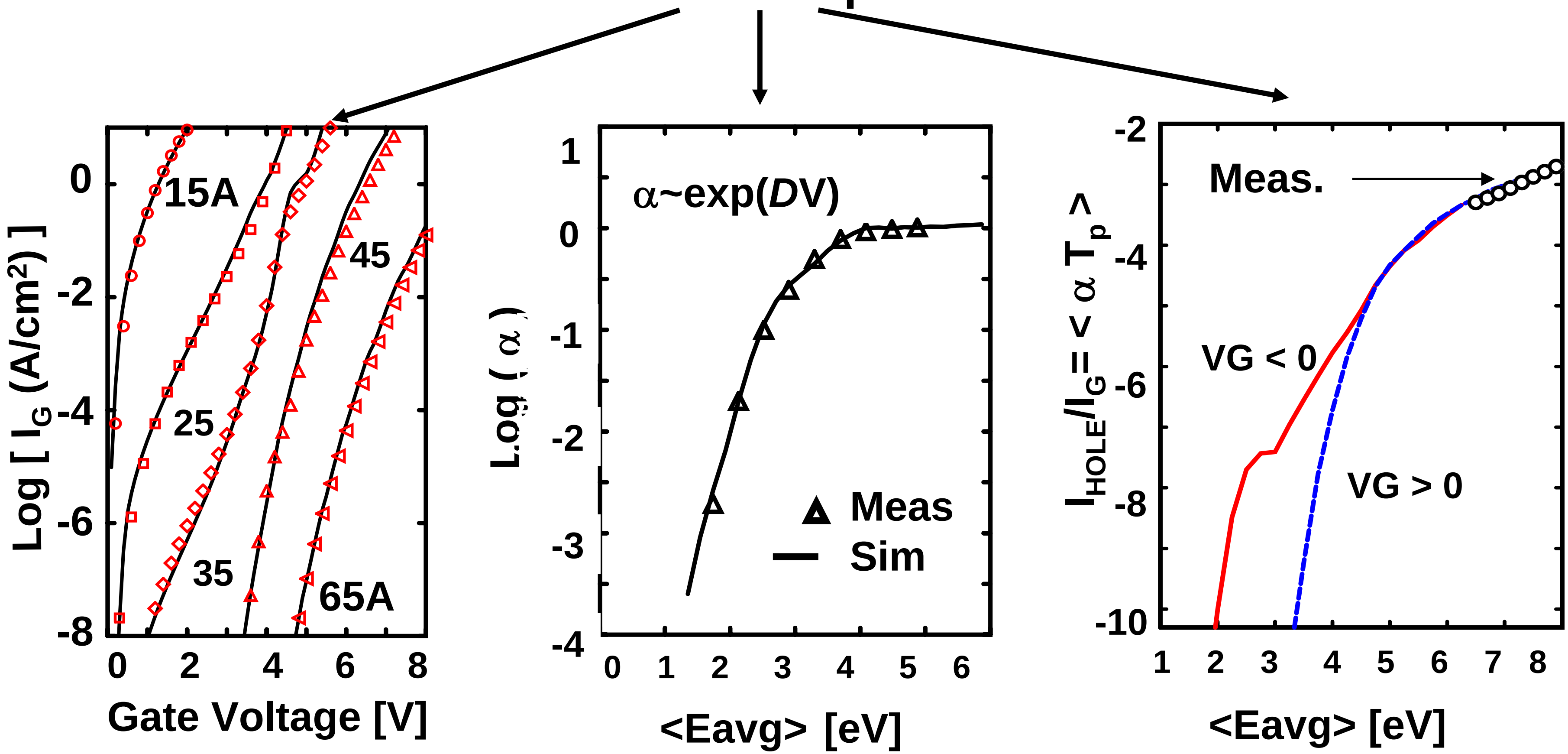
(probability that the hole will create a percolation defect)

N_{BD} - **Density of percolation defects at breakdown**

Ballistic transport and hot contacts … in 1980s!

AHI Model: Numerical Calculation

$$J_h = J_e \, \alpha \, T_p$$

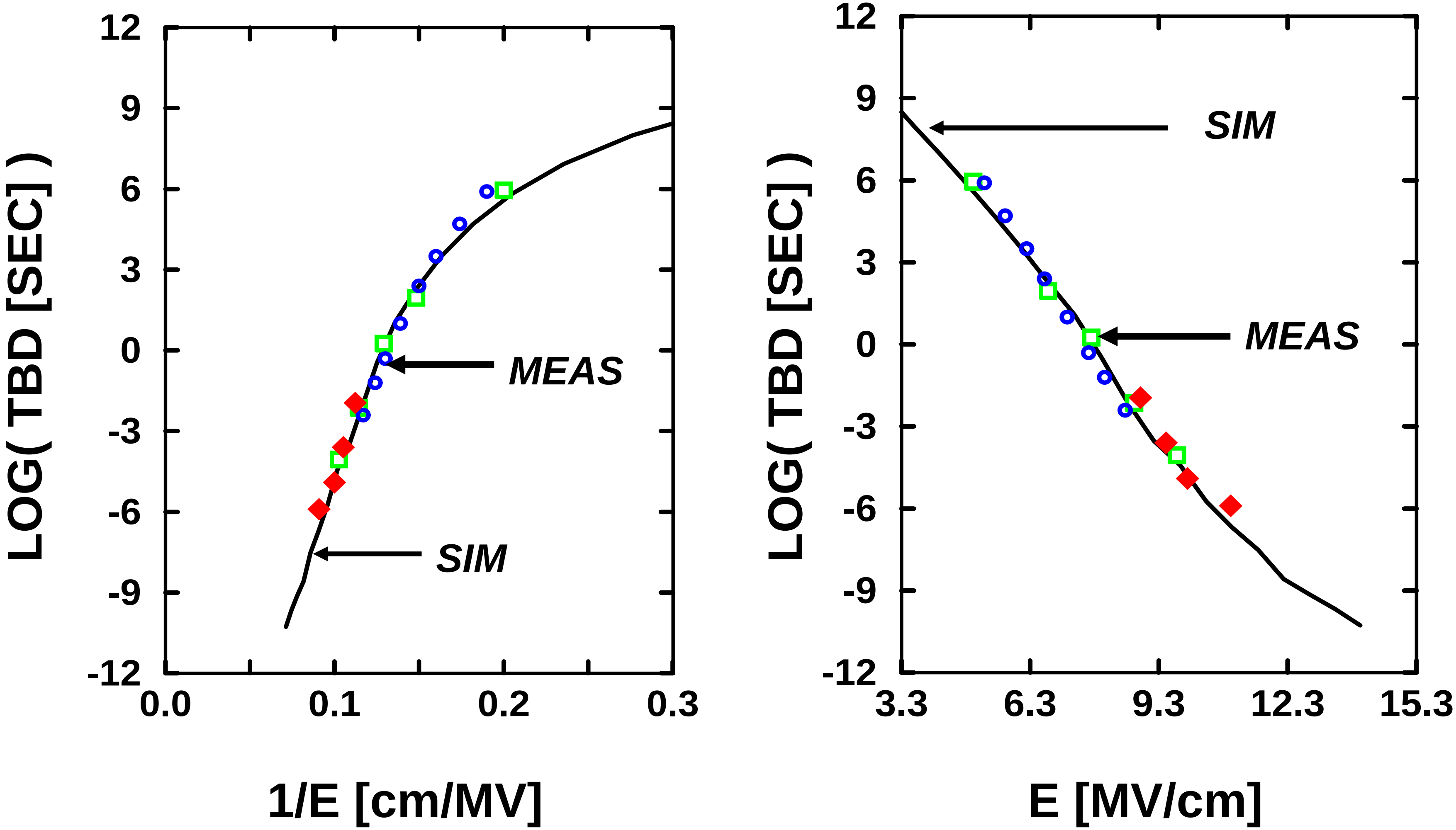


Ghetti, INFOS99
Lo, APL97

Bude (IEDM98)
Ezaki (SISC00)
Kamakura(IEDM99,JAP00))
Palestri(SISC00)

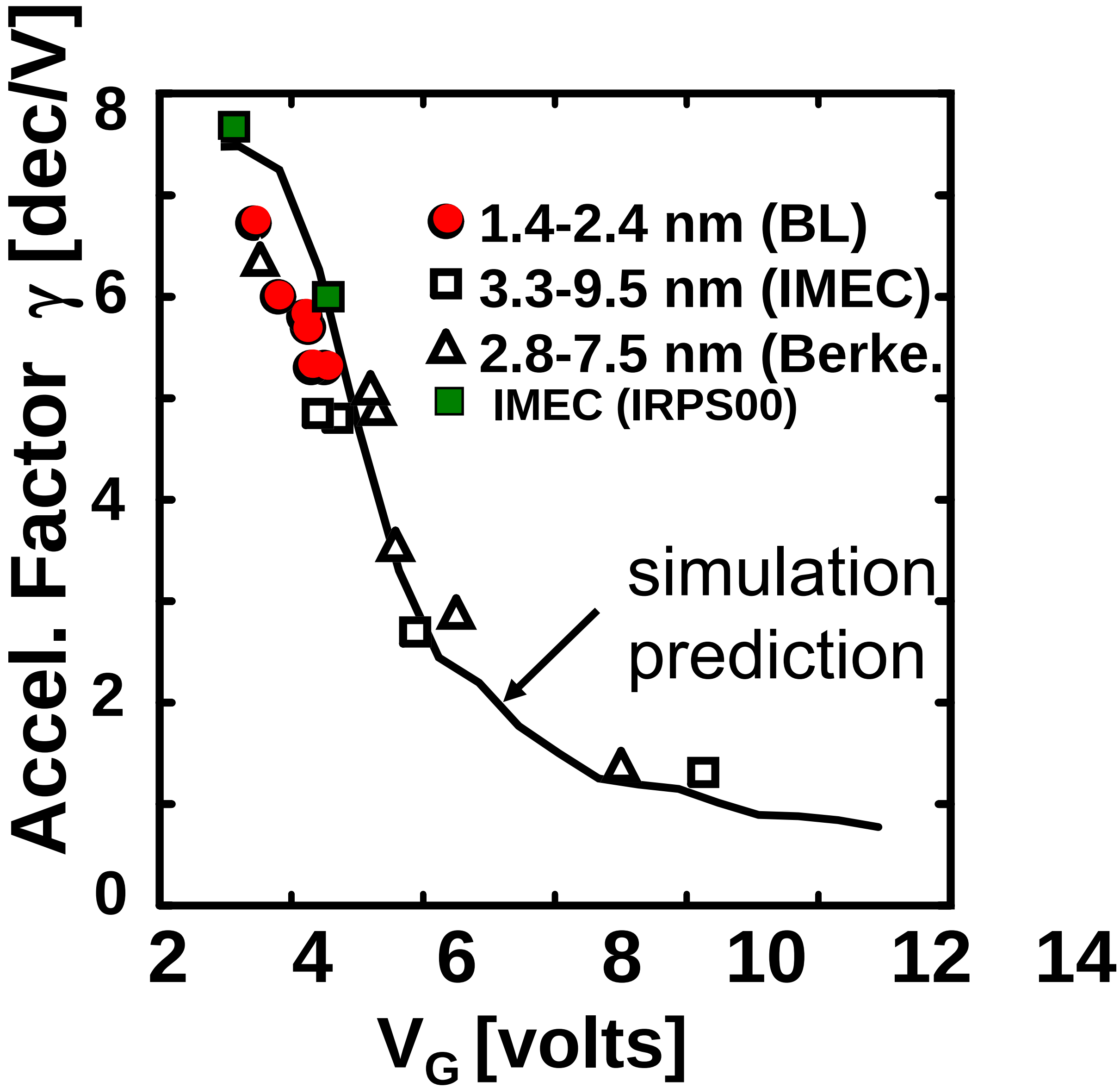
Bude(IEDM98)
Alam(IRPS00)
Palestri(SISC00)

Verification: Field Dependence

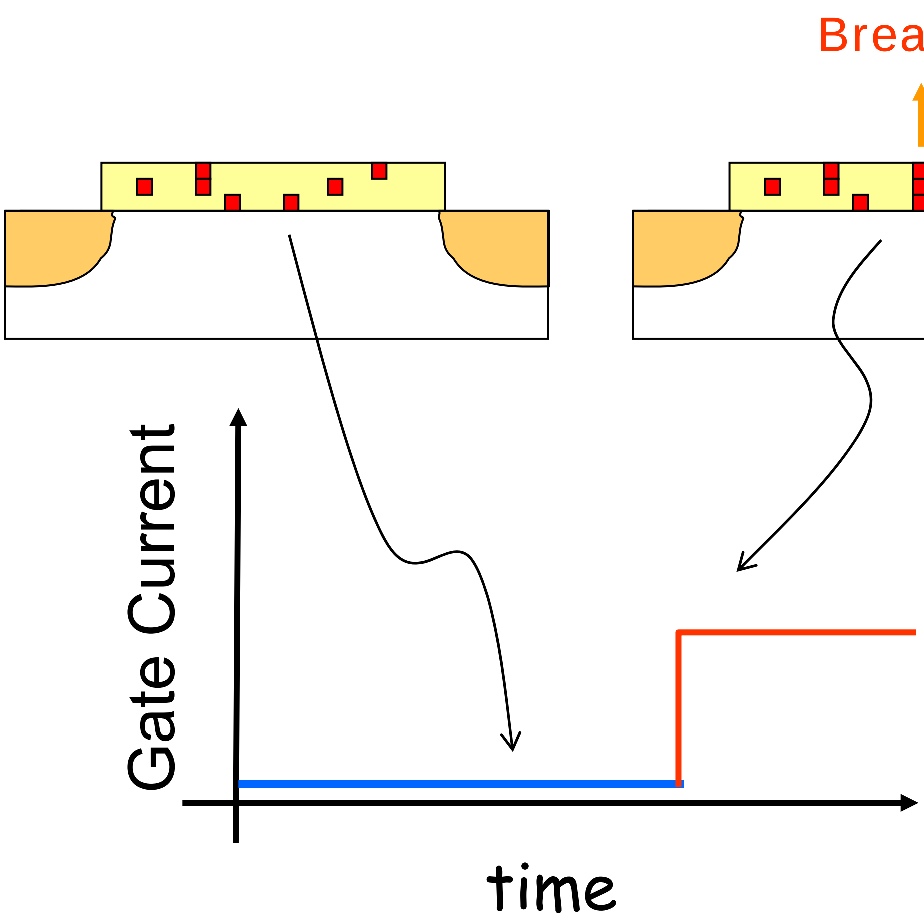


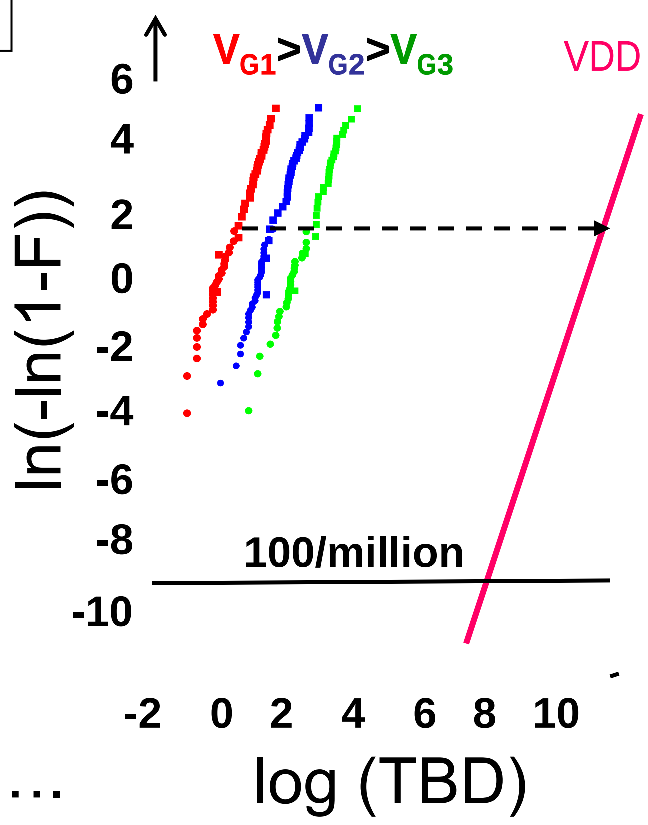
[Meas.] Hu, IEDM96, Teramoto, IRPS99, Yassine, APL99.

Reduced Defect Generation at Low Voltage



Mean Failure Time vs. Failure Time Distribution

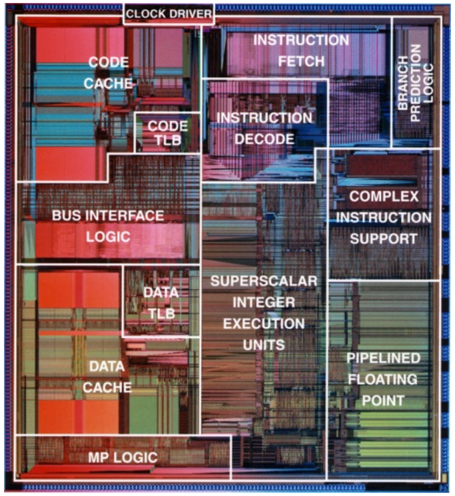




Average lifetime is not good enough ….

A difficult problem …

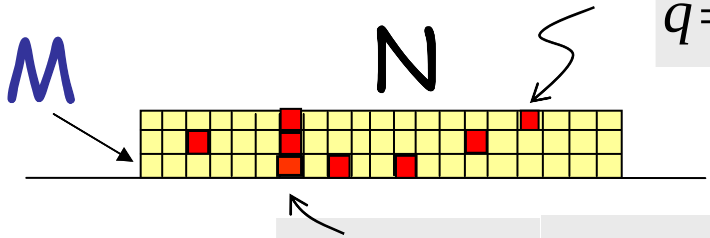
1 CPU ~ 10^8 -10^9 Transistors



When one transistor fails, so does the IC

Statistical distribution is very important ….

(Simple) Theory of Statistical Breakdown



$$q = \left(t/t_0\right)^{\alpha}$$

$$p = q^M = \left(t/t_0\right)^{M\alpha} \equiv \left(t/t_0\right)^{\beta}$$

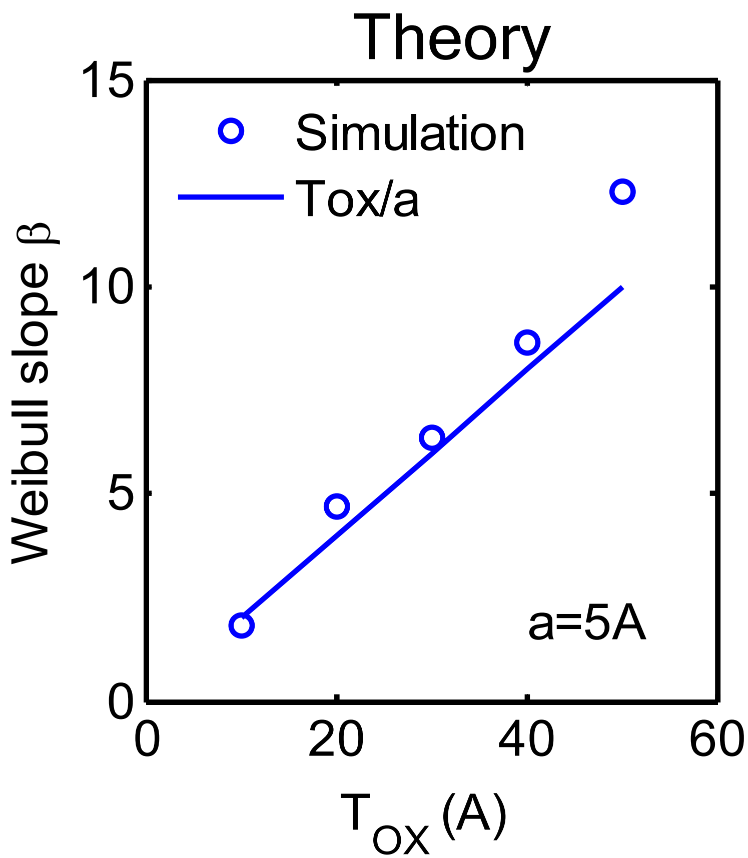
$$P_0 = (1-p)^N = (1-Np/N)^N = \exp(-Np)$$

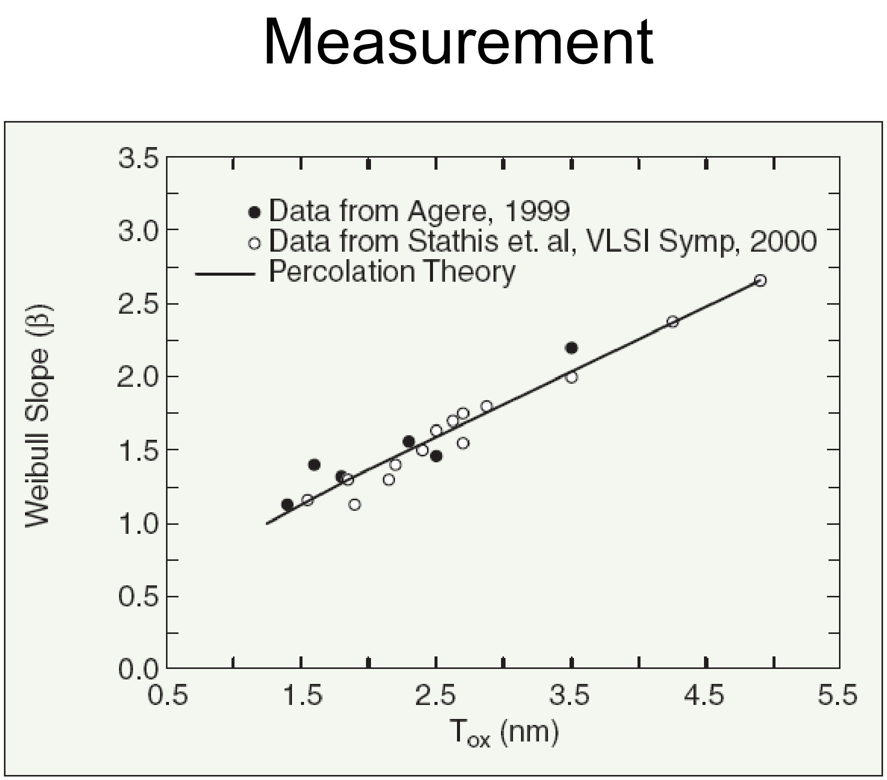
$$1 - F(p) = P_0 = \exp(-Np)$$

$$W \equiv \ln(-\ln(1-F)) = \beta \ln(t) - M\alpha \ln(t_0) + \ln(N)$$

If the bottom up view is correct, then we will have a straight-line in a Weibull plot and slope proportional to thickness

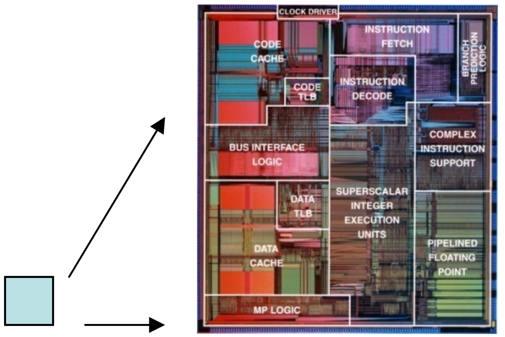
bottom-up prediction for oxide scaling





Thin oxide breaks much faster than thick oxide due to percolation, process-improvement can not solve this problem

Projection …



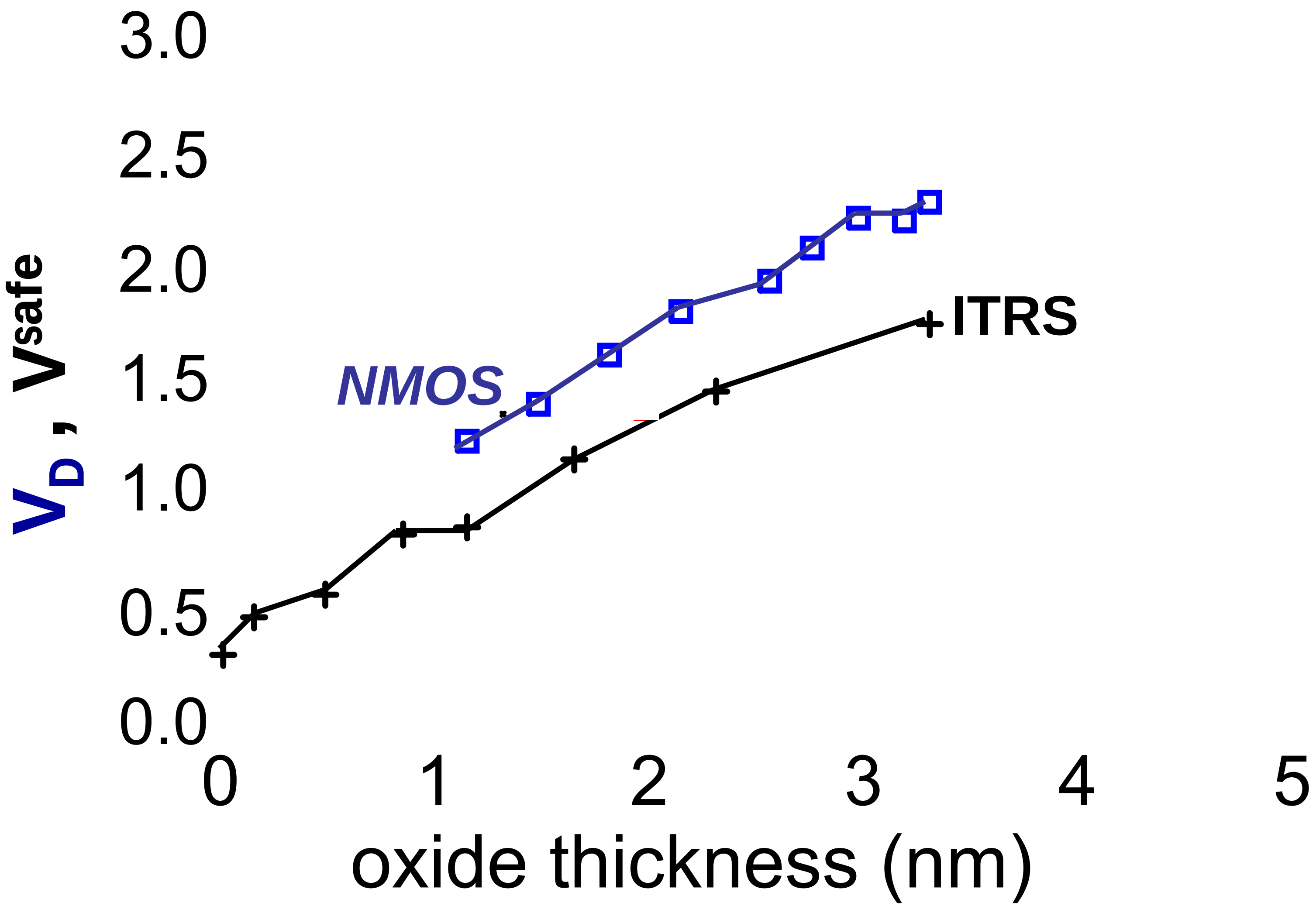
$$T_{BD}^{50\%}(A_{IC}) = (A_{TEST}/A_{IC})^{1/\beta}\; T_{BD}^{50\%}(A_{TEST})$$

$$T_{BD}^{q\%}(A_{IC}) = \left[\frac{\ln(1-q/100)}{\ln(1-0.5)}\right]^{1/\beta} T_{BD}^{50\%}(A_{IC})$$

$$V_{safe} = V_{test} - \log\left[\frac{10\text{ yrs}}{T_{BD}^{q\%}}\right] \Big/ \gamma_{V,acc}$$

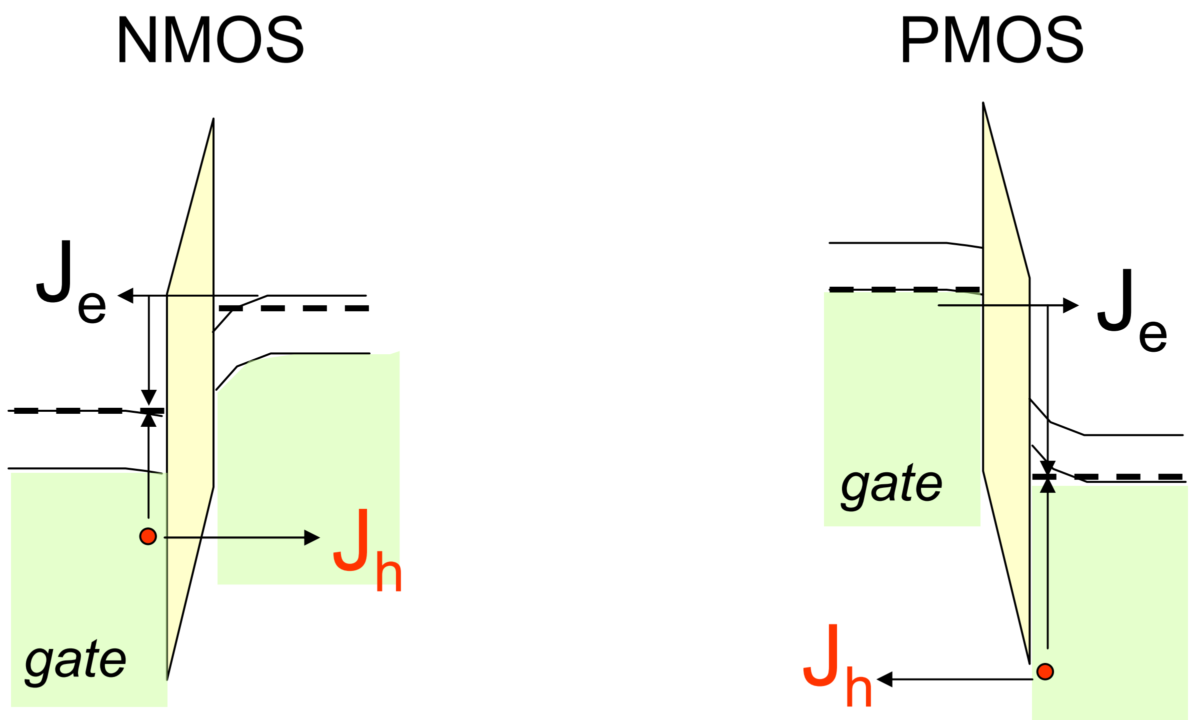
HW: Derive this equations based on the last 10 slides …..

NMOS Generally Reliable



PMOS vs. NMOS …

$T_{BD} \sim 1/J_h$ with $J_h = J_e \langle \alpha T_h \rangle$



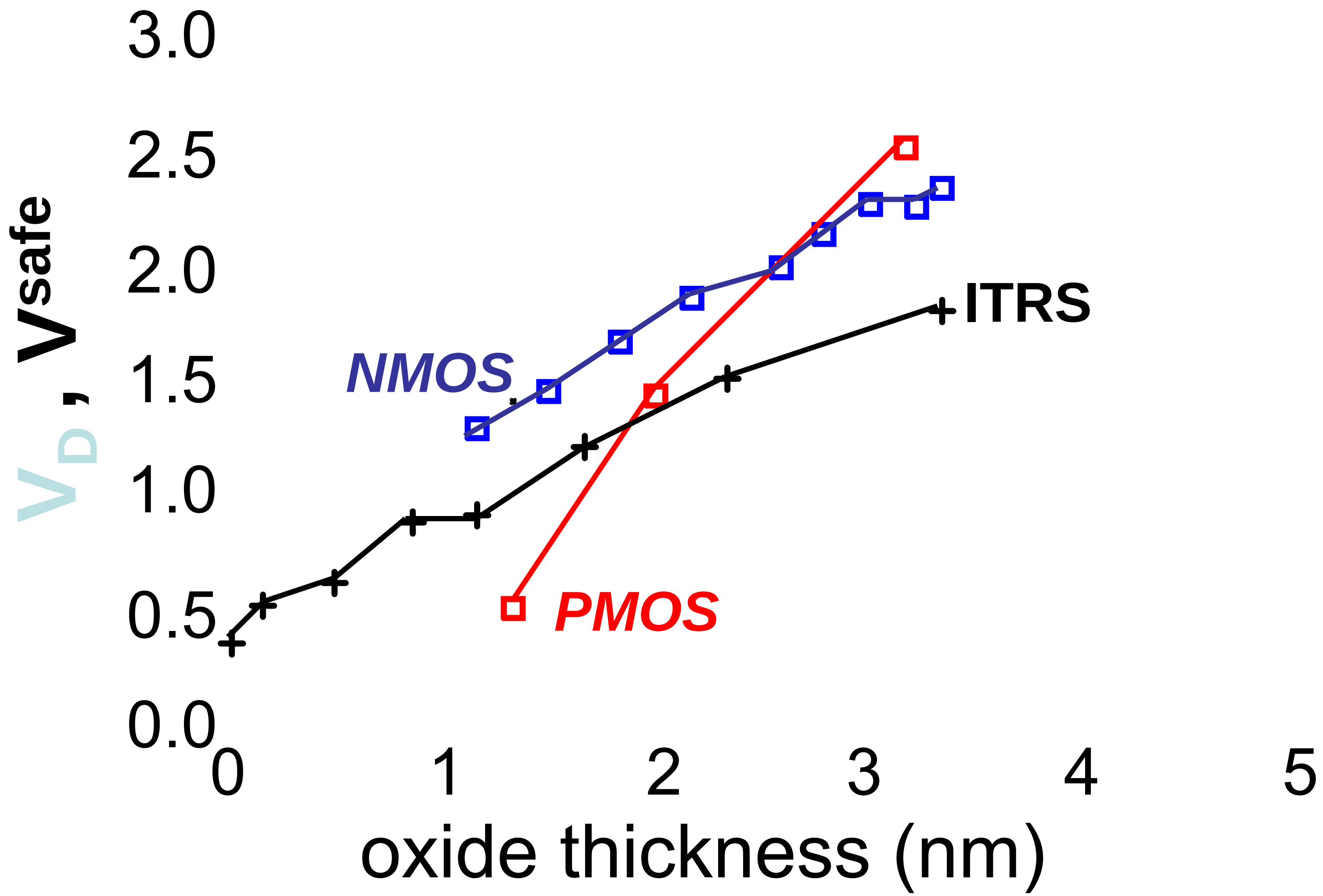
For oxide < 2 nm

$J_h^{PMOS} > J_h^{NMOS}$, so

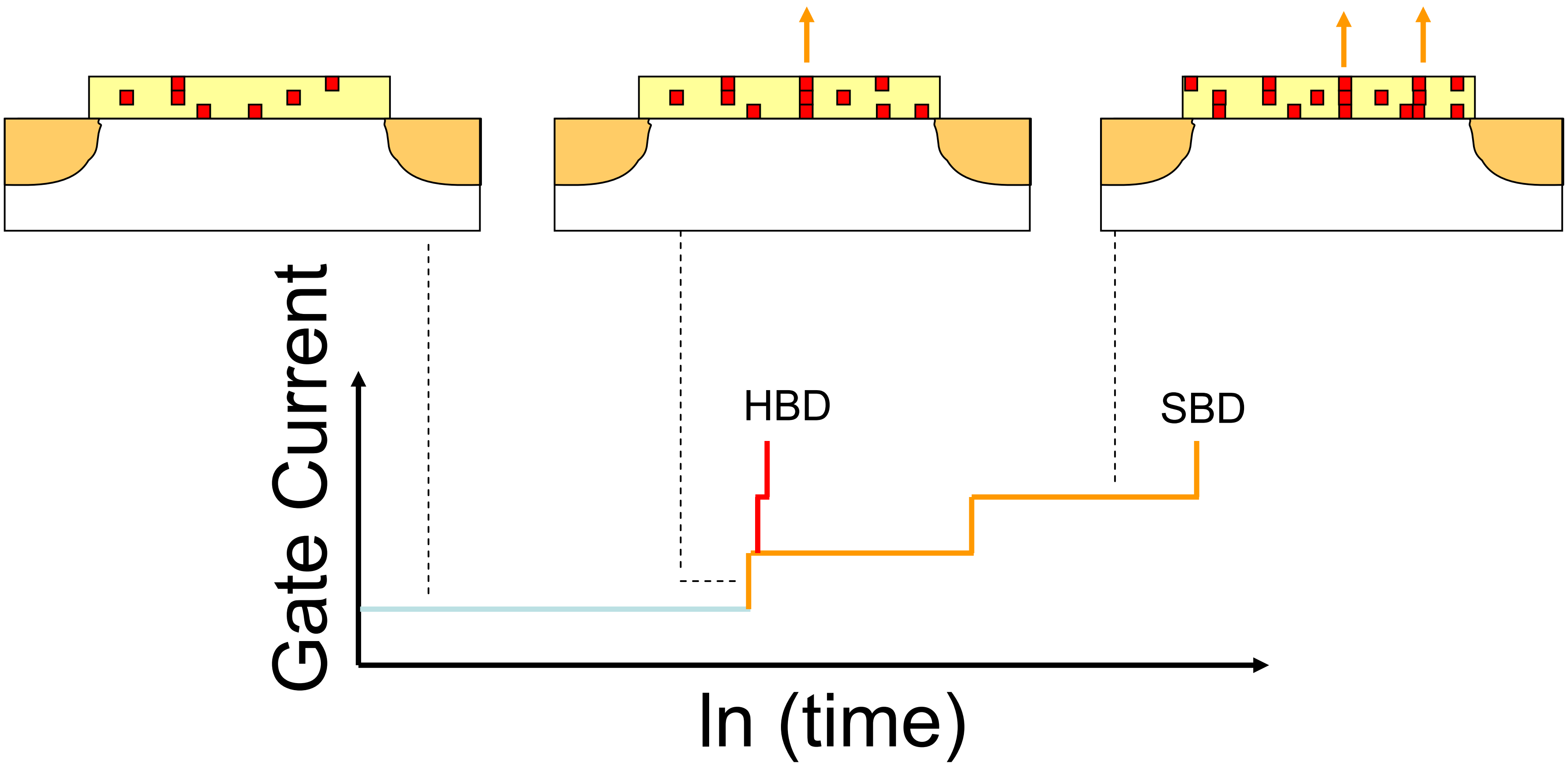
$T_{BD}^{PMOS} < T_{BD}^{NMOS}$

J. Bude, IEDM 98

What to do about PMOS?



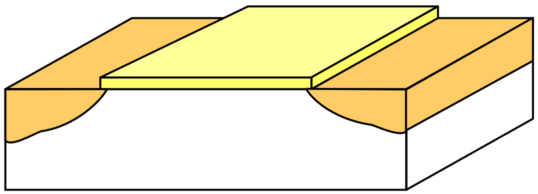
Hard vs. Soft Breakdown

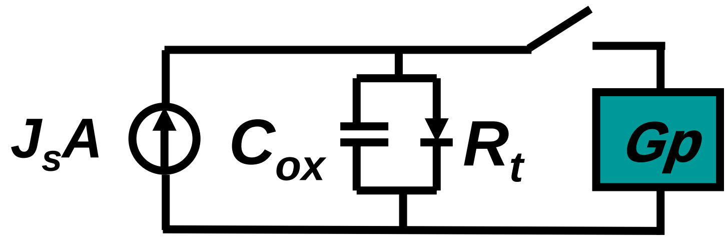


Q1: What are the statistics of soft breakdowns ?
Q2: What impact do these statistics have on reliability ?

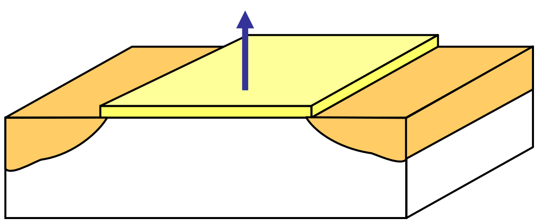
A Simple Model for Soft and Hard Breakdown

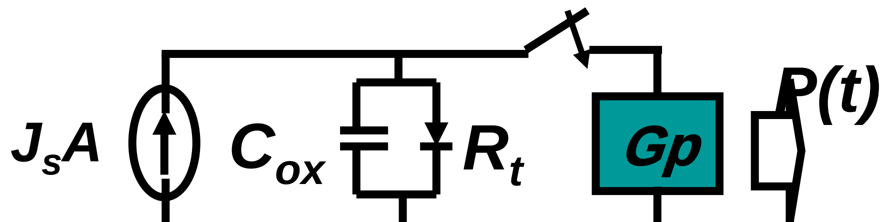
(a) t < TBD, only tunneling



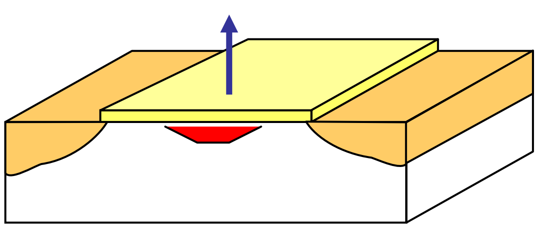


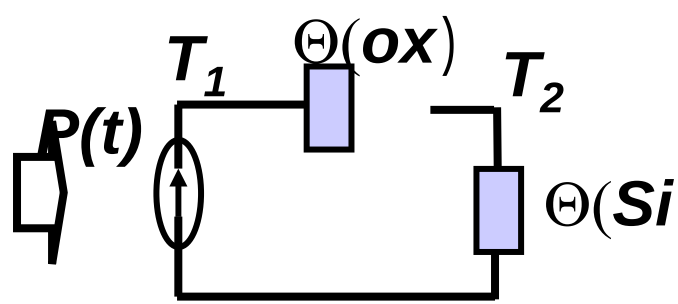
(b) t = TBD, BD current initiates





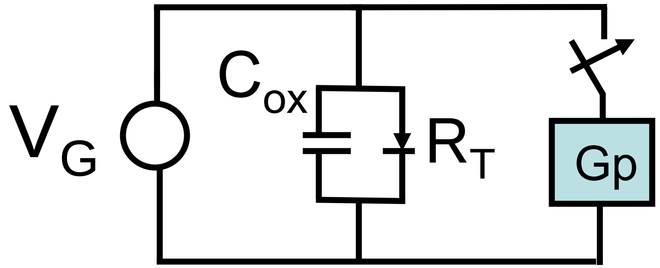
(c) t > TBD, transient heating



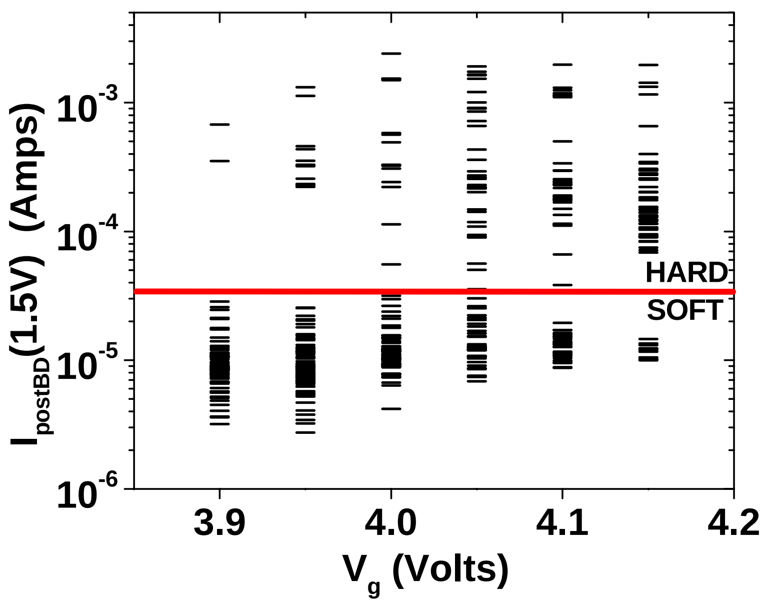


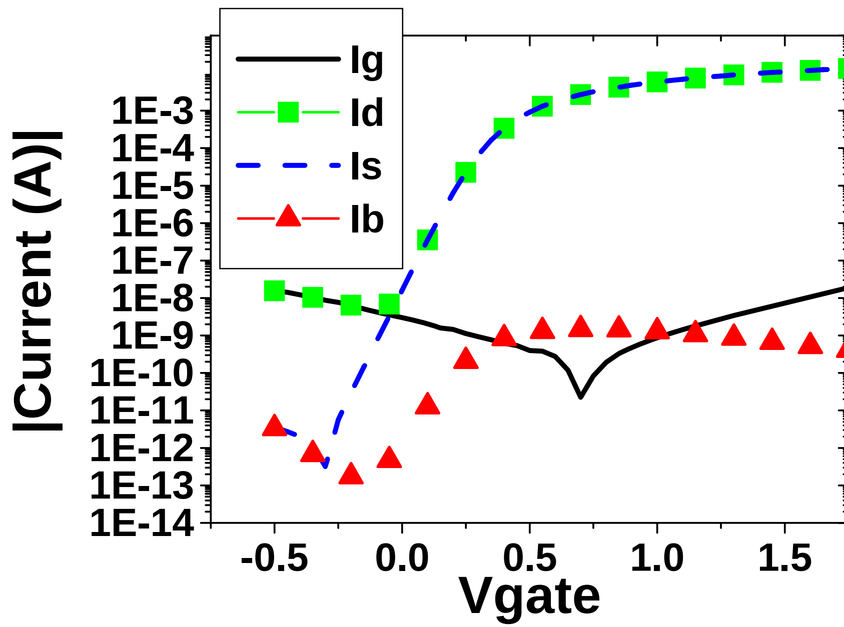
If P(t) below certain threshold, breakdown will be soft

Soft Breakdown at Reduced Voltage



$$P = G_p V_G^2$$

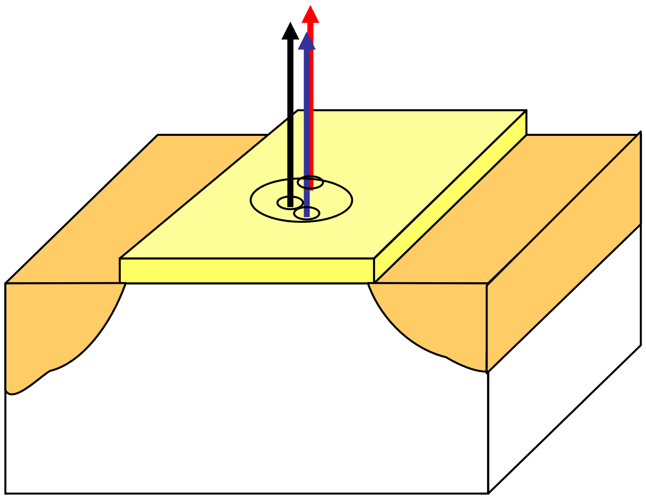




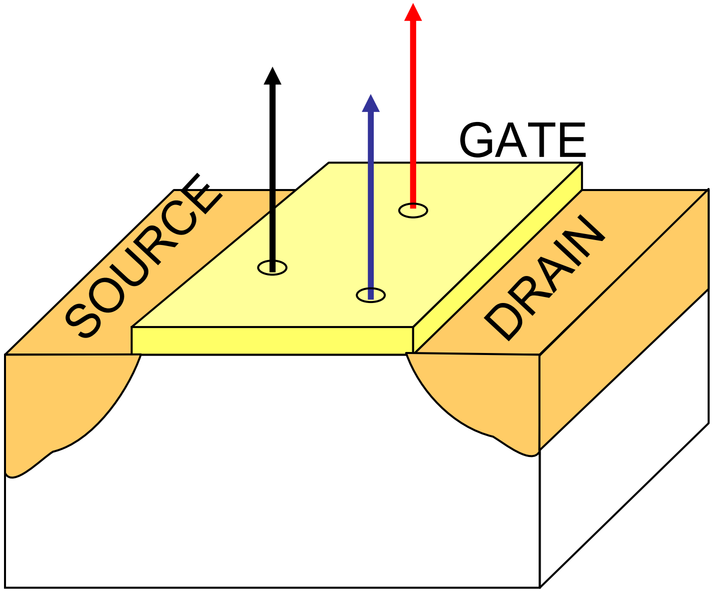
Expt. Evidence of SBD @ low VGPerformance unaffected by SB

Characteristics of Hard and Soft Breakdown

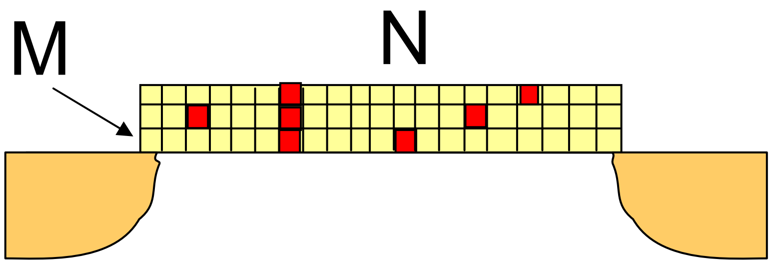
Hard Breakdown



Soft Breakdown



Statistics of Soft Breakdown



Prob. of a filled column: $p = q^M$

Prob. of filled cell: $q=(at^{\alpha}/NM)$

Prob. of exactly n-SBD

$$P_n = {}^{N}C_n\, [p^n]\, [(1-p)^{(N-n)}]$$

$$P_n = (\chi^n/n!) \exp(-\chi)$$

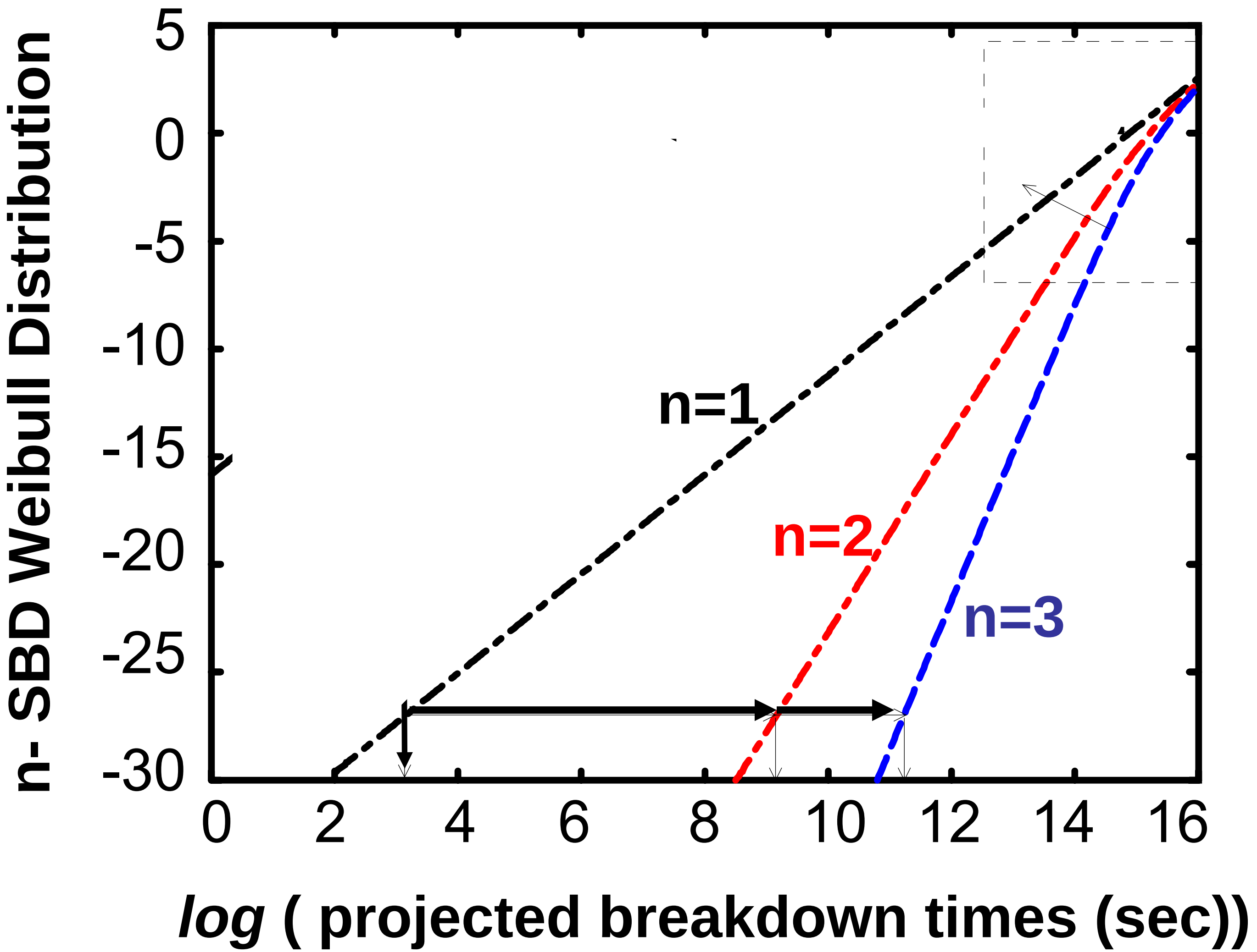
with $\chi=(t/\eta)^{\beta}$ and $\beta=M\alpha$

Prob. of >= n SBD

$$F_n(\chi) = 1 - \sum_{k=0}^{n-1} P_k(\chi)$$

measured data: $W_n = \ln[-\ln(1-F_n)]$

Lifetime Improvement

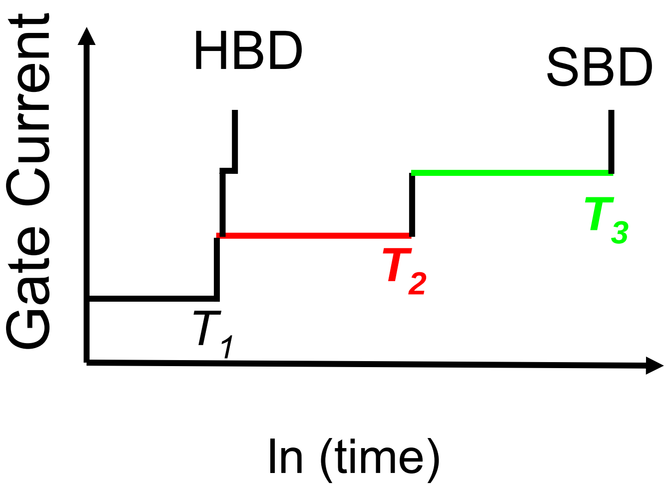


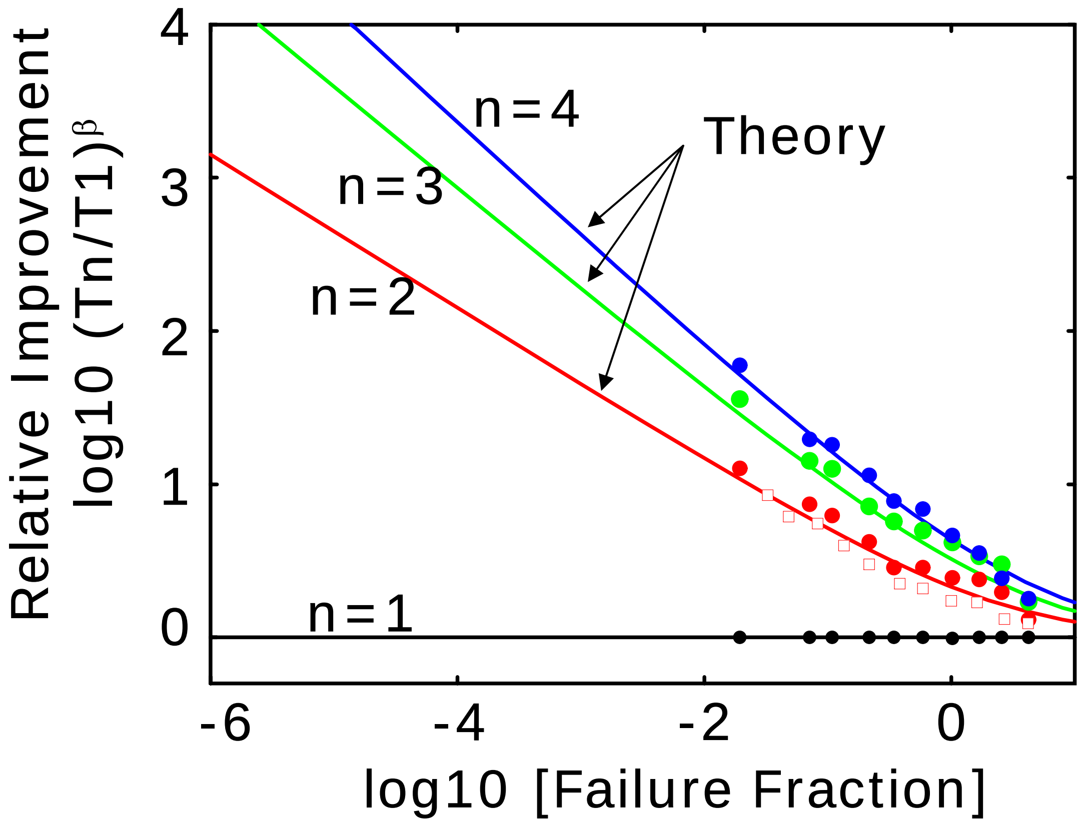
100 million Transistors

1 part per 10^4 failure

SBD Improves Lifetime Geometrically …

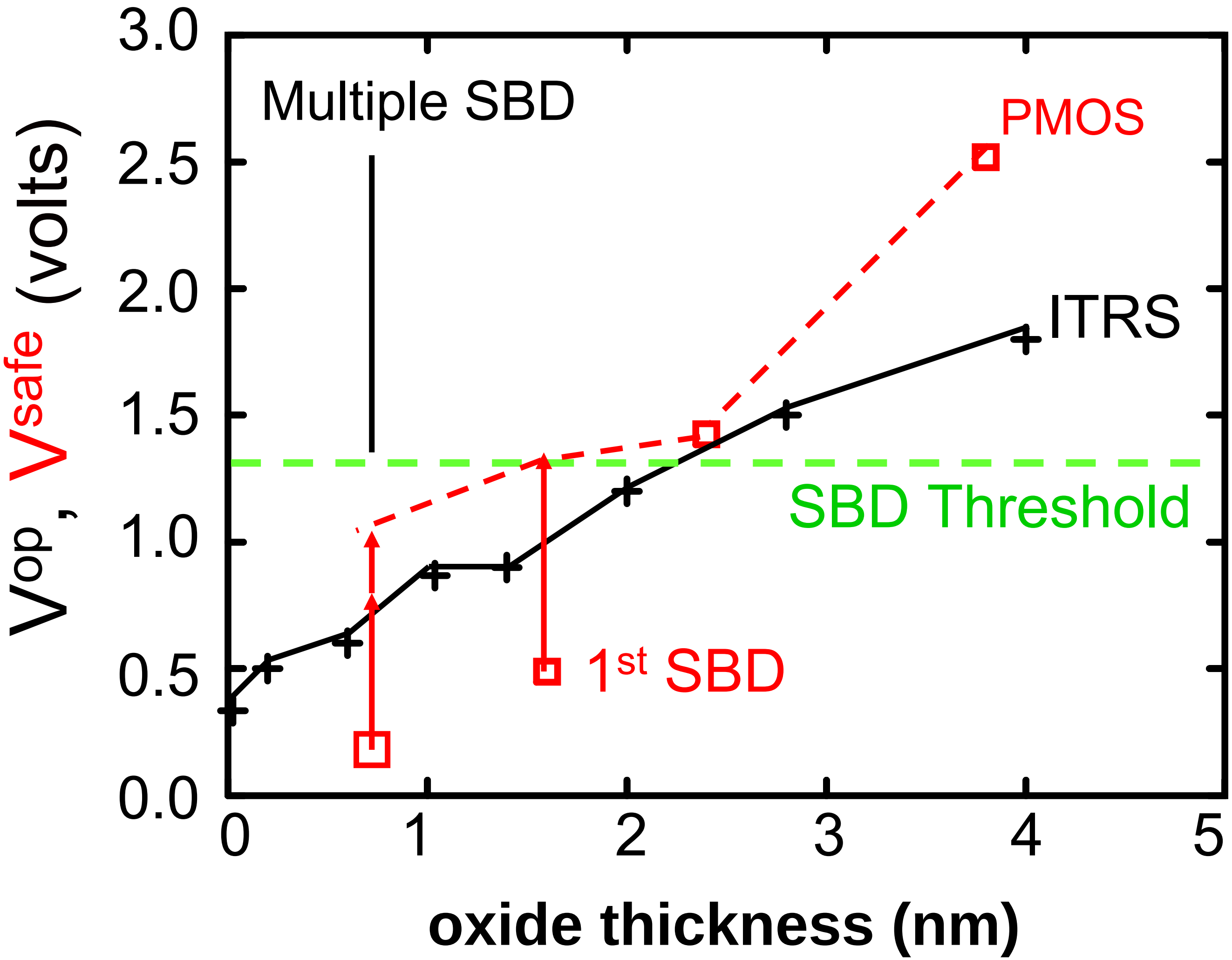
$$(T_n / T_1)^{\beta} = (n/e)(2\pi n)^{1/2n} / F_n^{(1-1/n)}$$



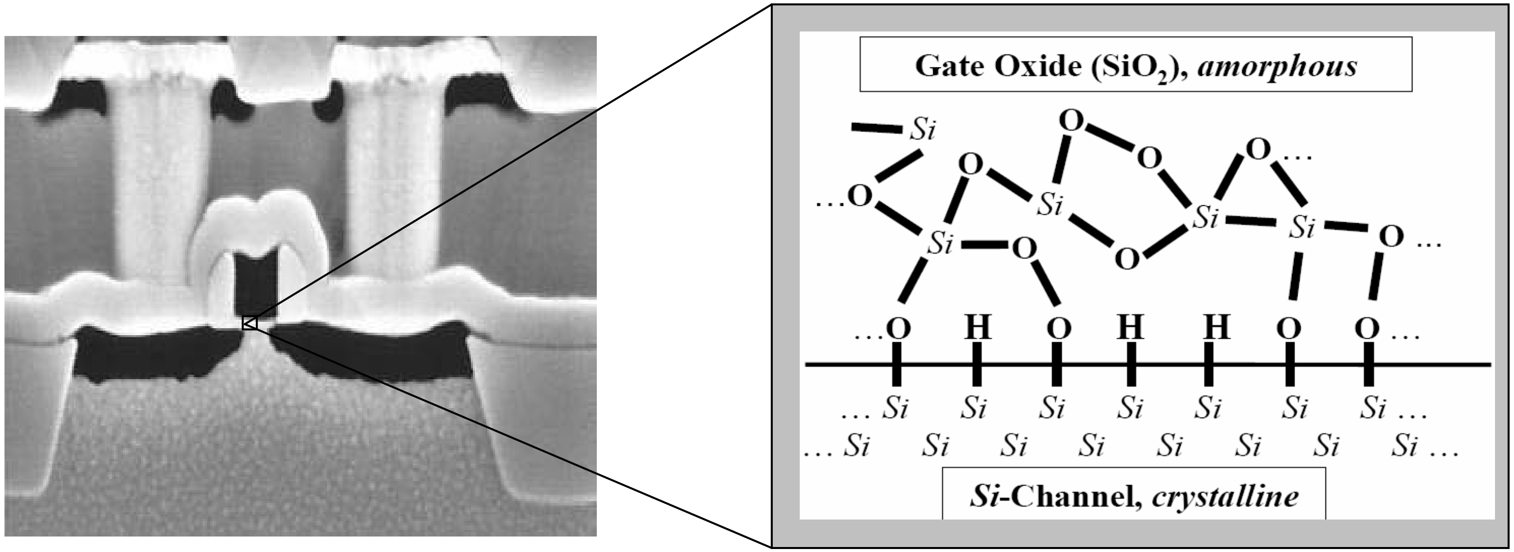


Alam, Nature, 2003

PMOS Reliability with SBD



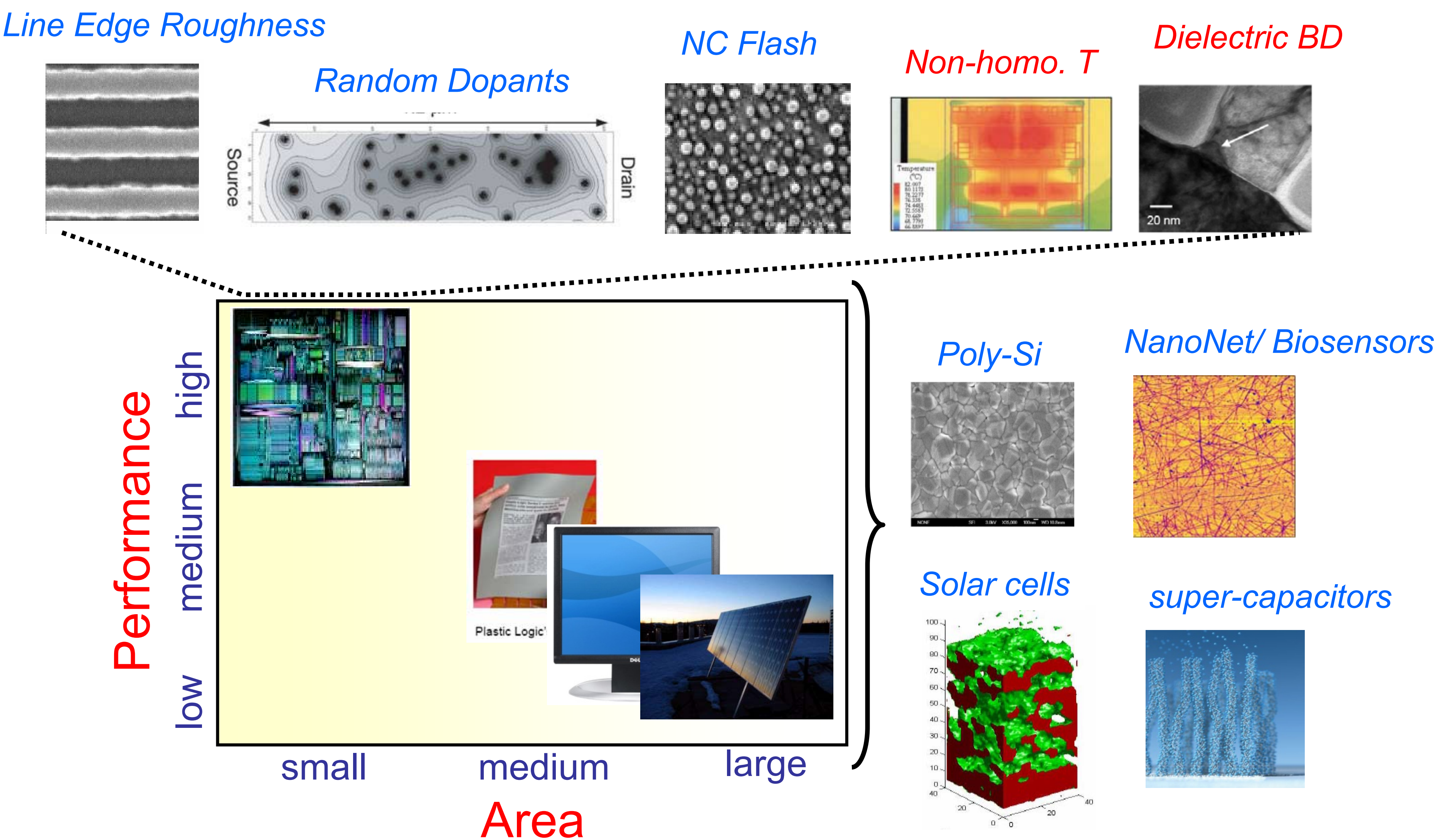
The topics we did not talk about …



Broken Si-H bonds
- Negative Bias Temperature Instability (NBTI)
- Hot carrier degradation (HCI)

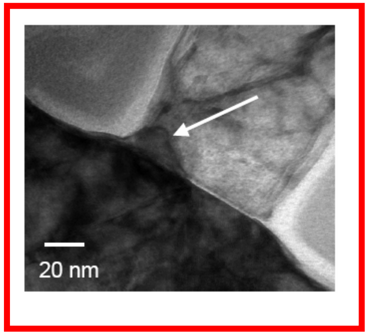
Broken Si-O bonds
- Gate dielectric Breakdown (TDDB)
- Electrostatic Discharge (ESD)
- Radiation induced Gate Rupture (RBD)

Spatial/Temporal Parameter Fluctuation



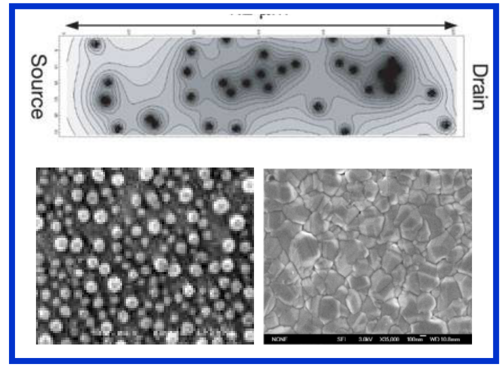
Process Fluctuation/ Reliability

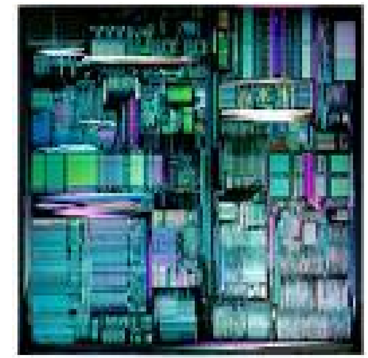
Reliability



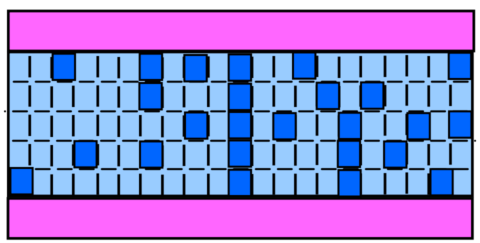
plus

Process

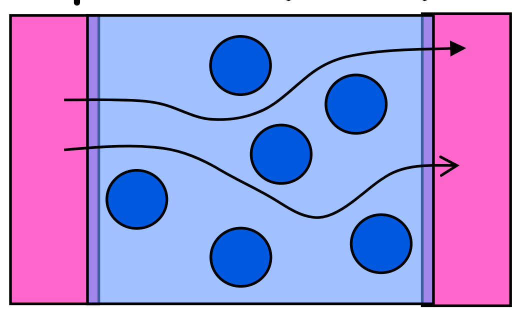




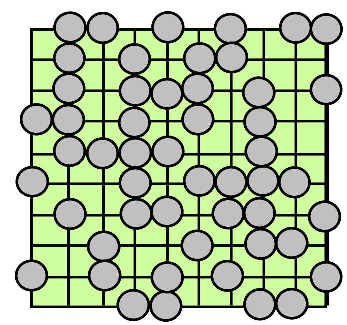
Side view (TDDB)



top view (RDF)



model



Spatial and temporal fluctuation should be considered with same framework …

More Information

Course

Reliability Physics of Nanoelectronic Devices
http://cobweb.ecn.purdue.edu/~ee650/
Contains lecture notes, programs, homework problems, references
www.nanohub.org
For videotaped lectures, tutorials, and programs

Journals

IEEE Trans. on Electron Devices
IEEE Trans. On Material and Device Reliability
Microelectronics Reliability

Conferences

International Electron Device Meeting
International Reliability Physics Symposium