



ECE606: Solid State Devices

Lecture 32: MOS Electrostatics

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Outline

1. Background

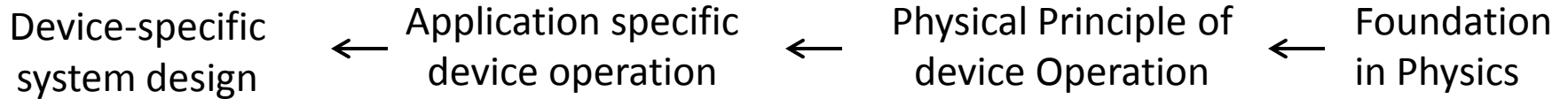
2. Band diagram in equilibrium and with bias

3. Qualitative Q-V characteristics of MOS capacitor

4. Conclusion

REF: Chapters 15-18 from SDF

Outline of the Course



TFT for Displays
CMOS-based Circuits for mP
LASERS for Disk Drives
MEMS for Read heads

Resistors (5 wk)
Diodes (3 wk)
Bipolar (3 wk)
MOSFETs (3 wks)

EE606

Quantum Mechanics + Statistical Mechanics
↓
Transport Equations

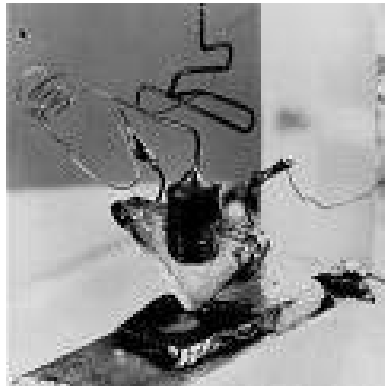
Scaling of MOSFETs

Vacuum
Tubes



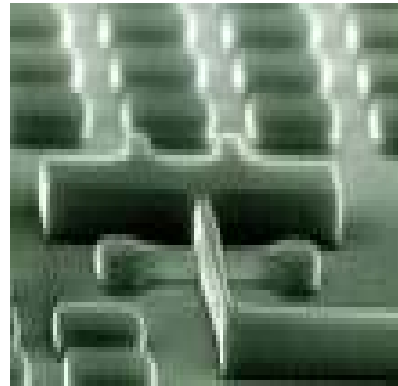
1906-1950s

Bipolar



1947-1980s

MOSFET



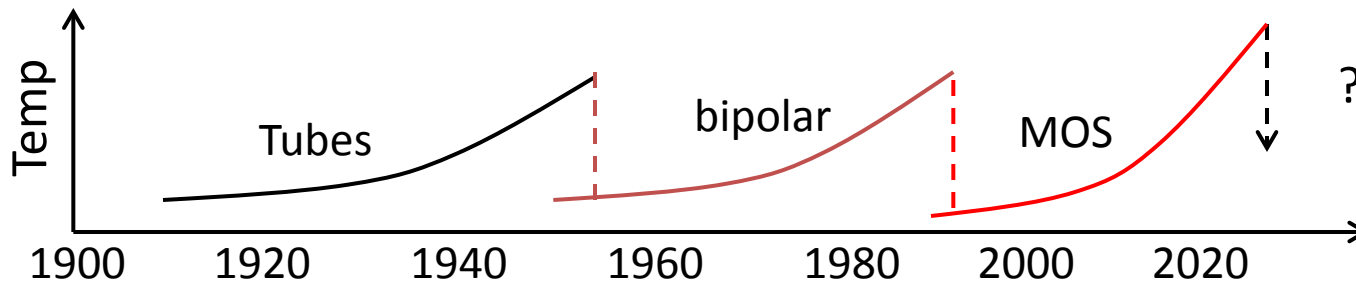
1960-until now

Now ??

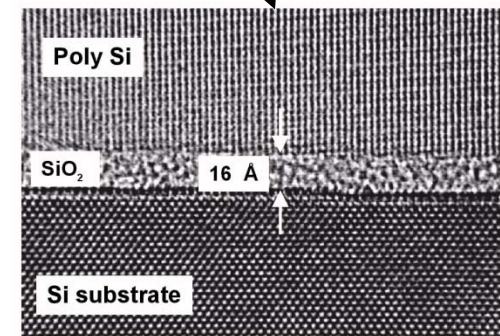
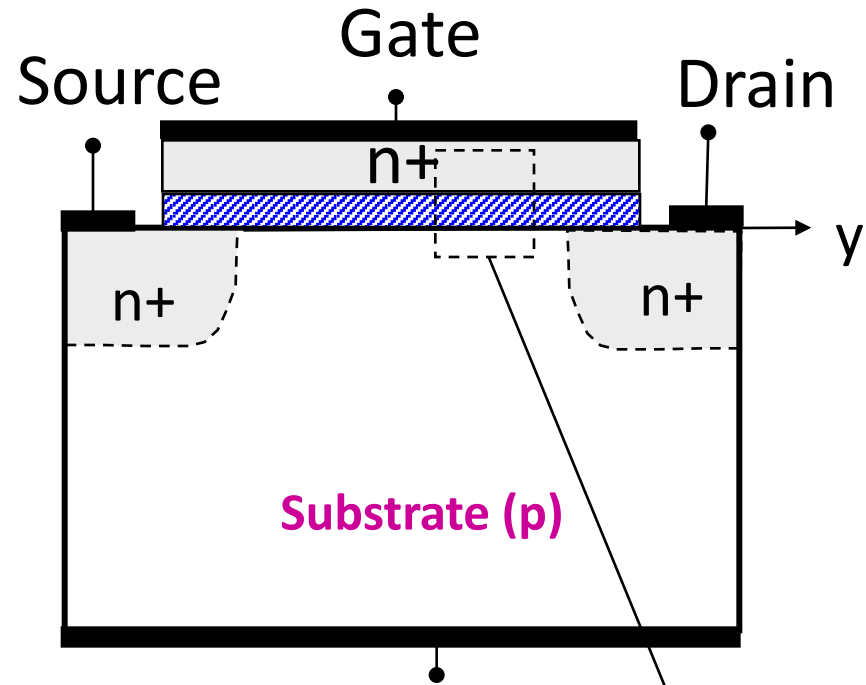
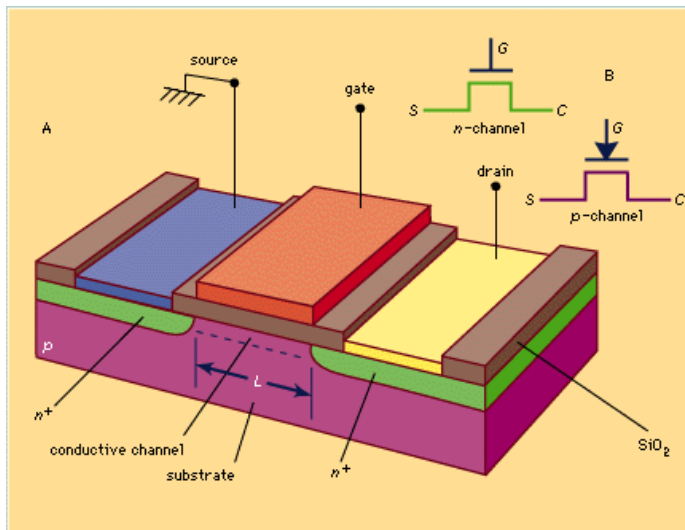
Spintronics

Bio Sensors

Displays

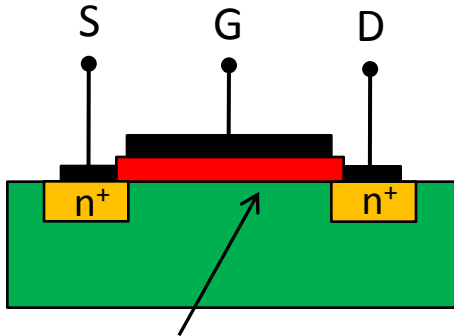


Basic Configuration of a MOSFET

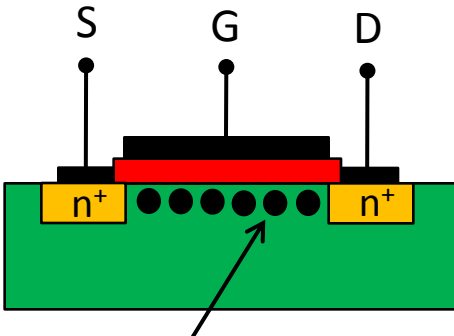
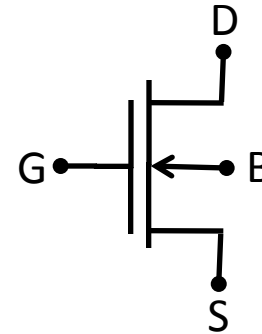


Almost like a lateral bipolar transistor!

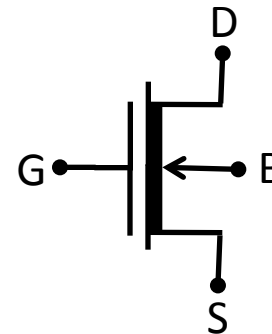
Symbols



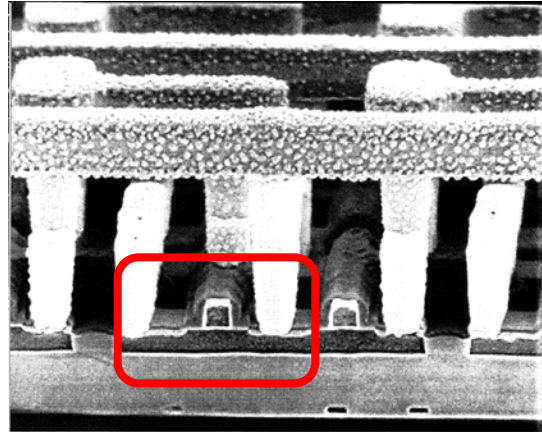
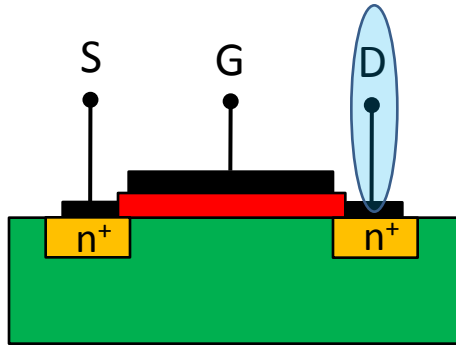
No channel
when $V_G = 0$



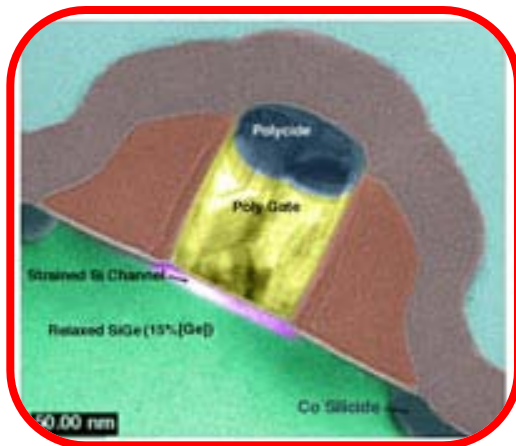
Channel
when $V_G = 0$



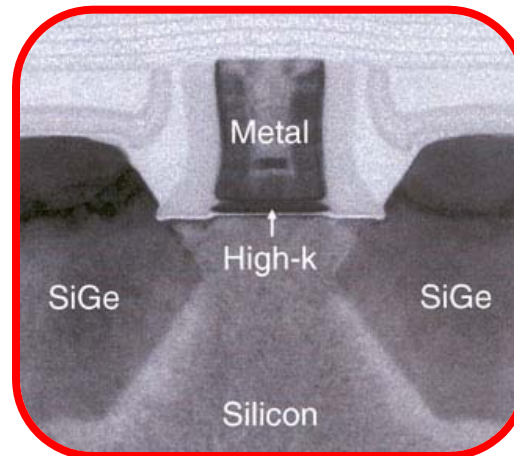
Background



Strained MOSFET



High-k/metal gate MOSFET

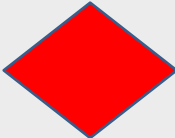


Sources:
IBM J. Res. Dev.
Google Images
Intel website

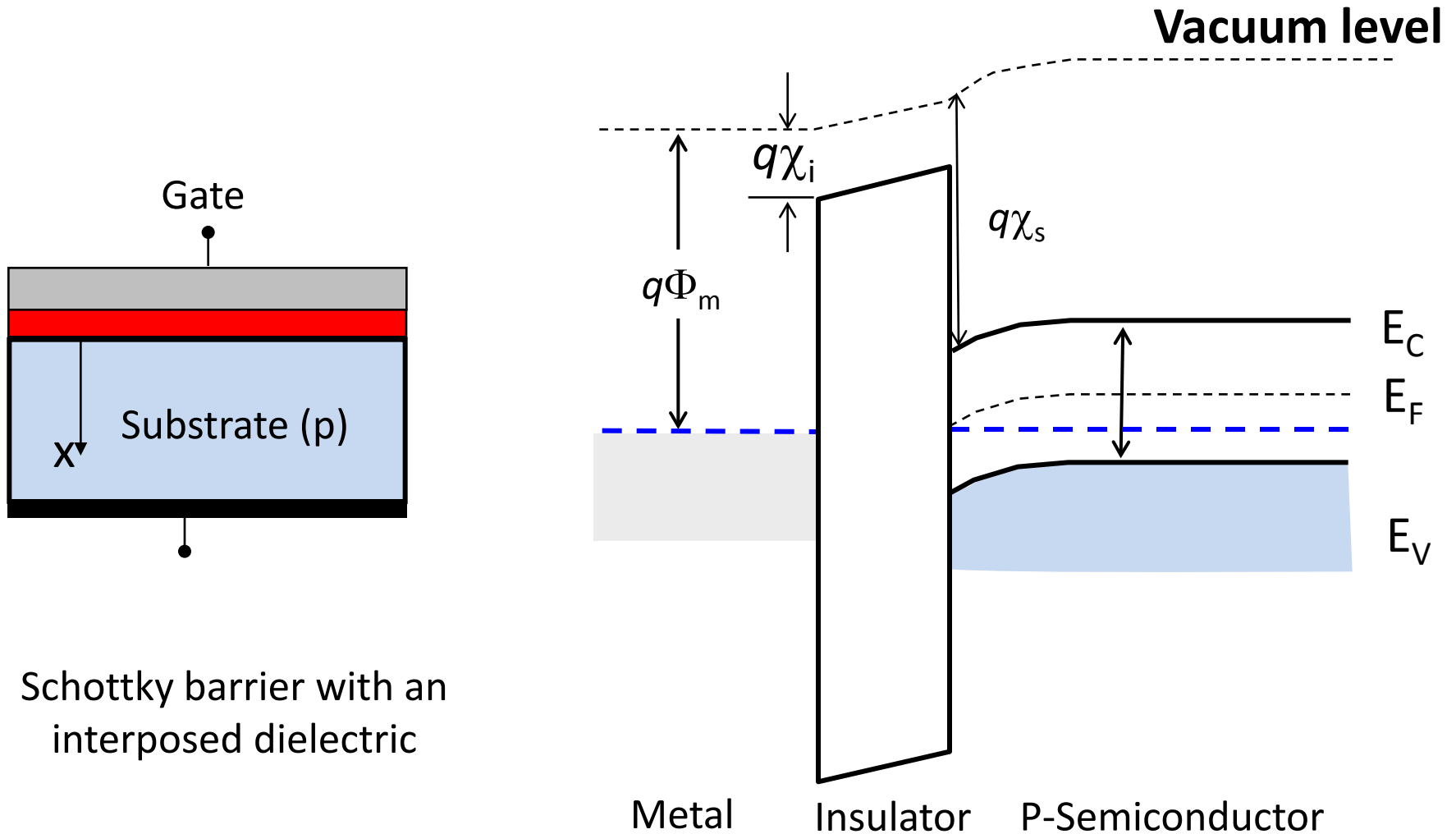
Outline

1. Background
- 2. Band diagram in equilibrium and with bias**
3. Qualitative Q-V characteristics of MOS capacitor
4. Conclusion

Topic Map

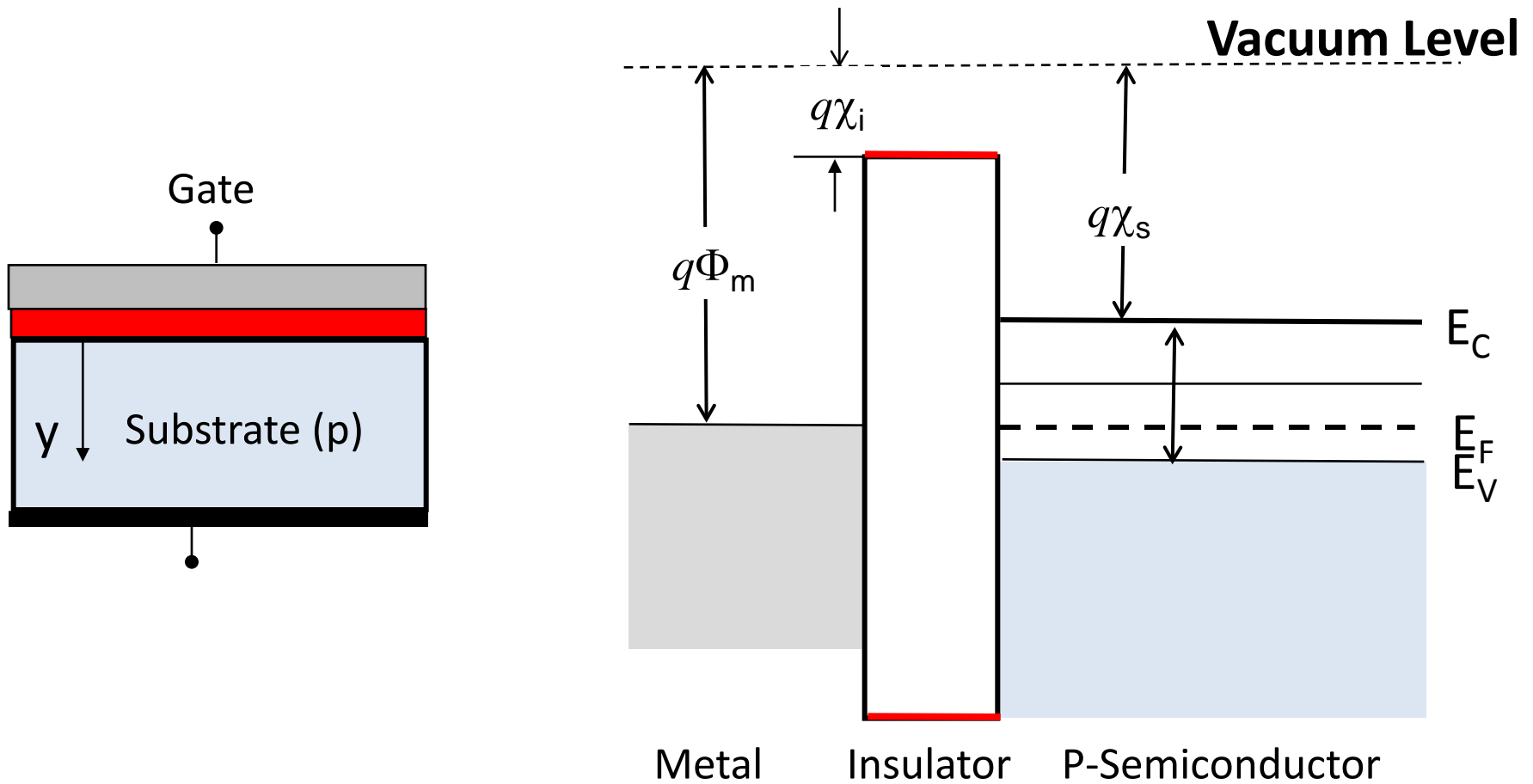
	Equilibrium	DC	Small signal	Large Signal	Circuits
Diode					
Schottky					
BJT/HBT					
MOS					

Electrostatics of MOS Capacitor in Equilibrium

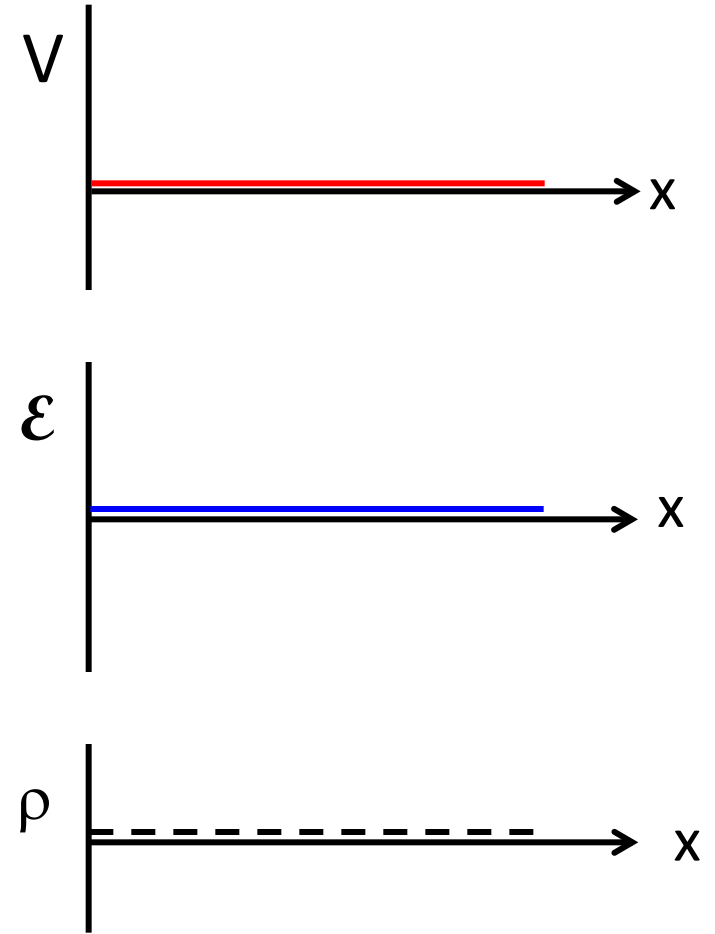
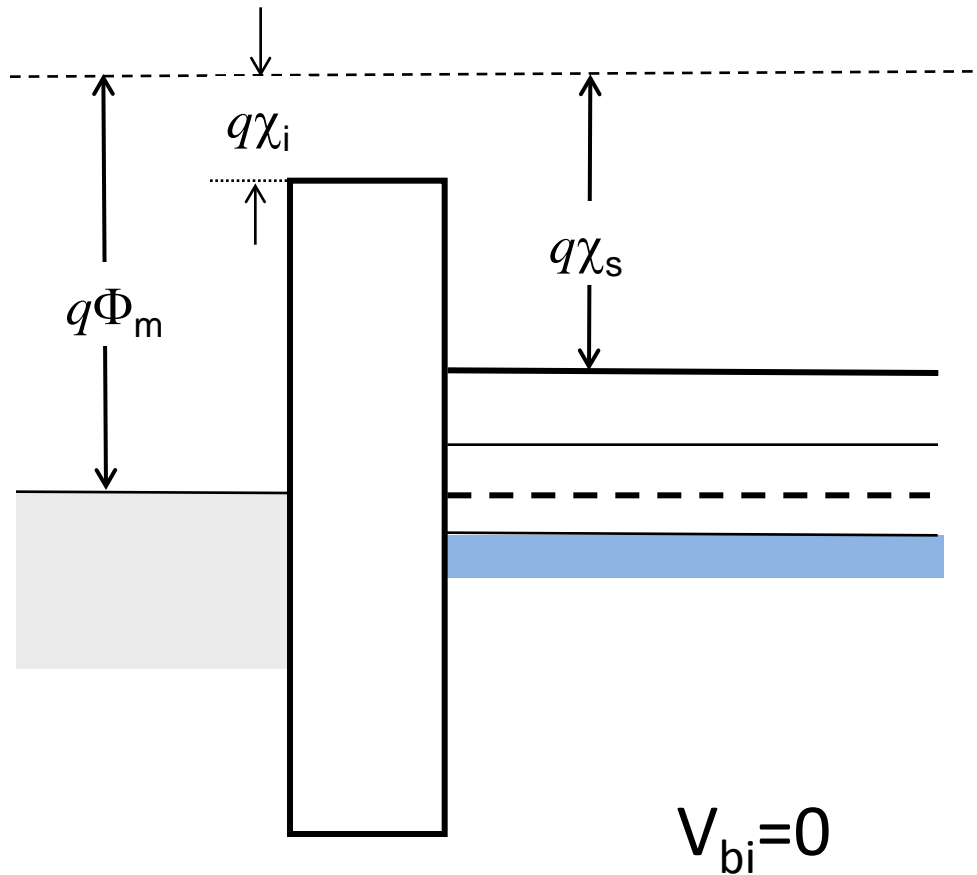


Schottky barrier with an interposed dielectric

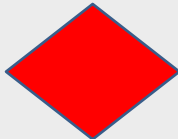
Idealized MOS Capacitor



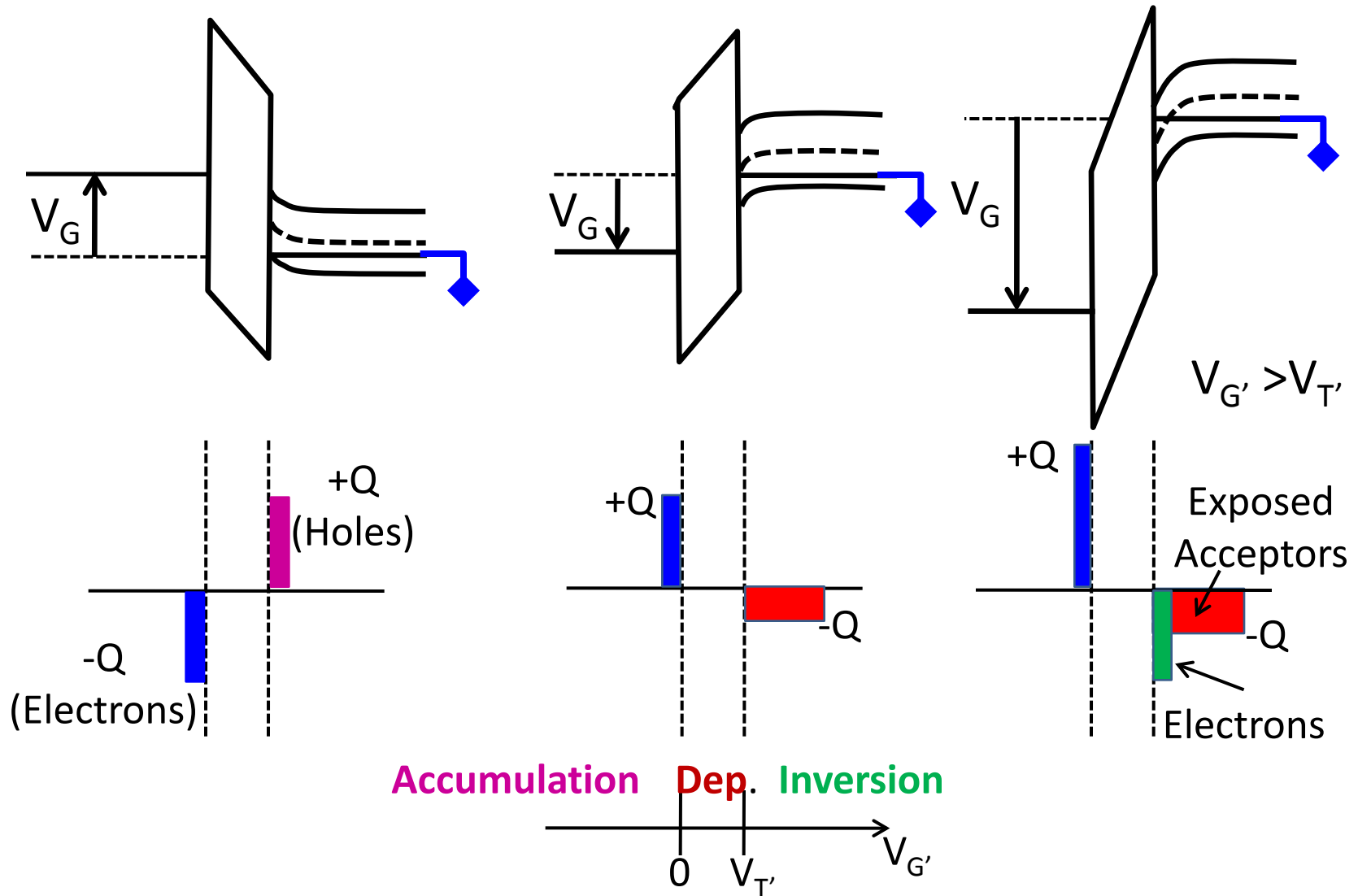
Potential, Field, Charges



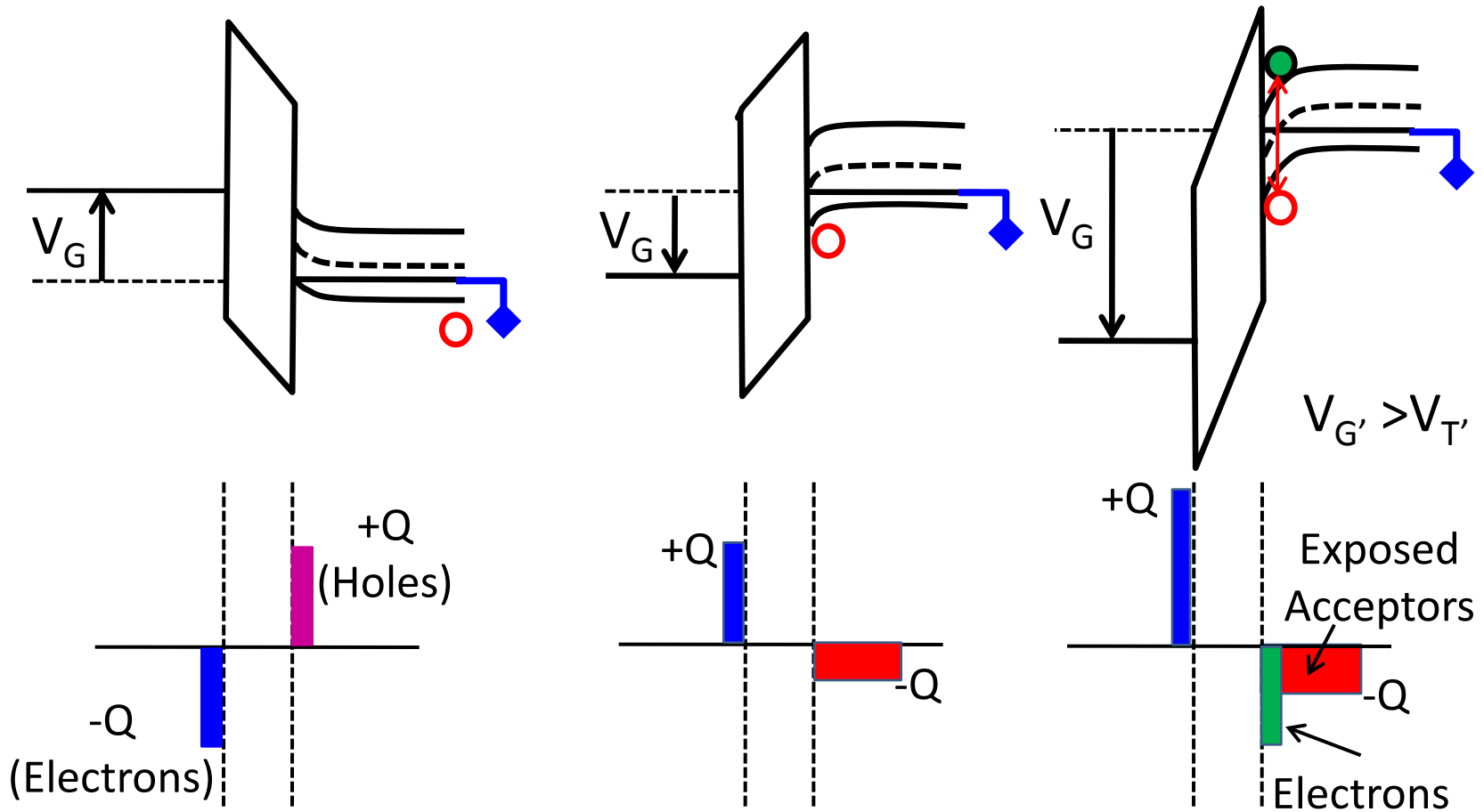
Topic Map

	Equilibrium	DC	Small signal	Large Signal	Circuits
Diode					
Schottky					
BJT/HBT					
MOSCAP					

Electrostatics under Bias

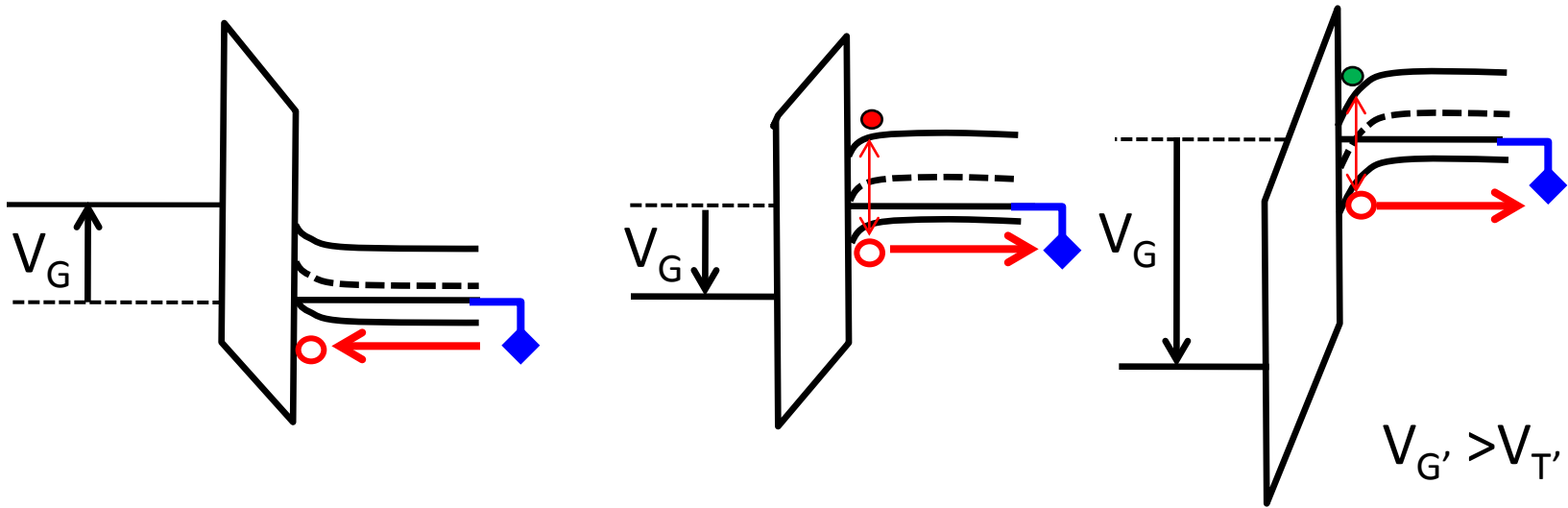


Where do charges come from?



- Integrate charge to find potential.

Response Time



Dielectric Relaxation

$$\tau = \frac{\sigma}{\kappa_s \epsilon_0}$$

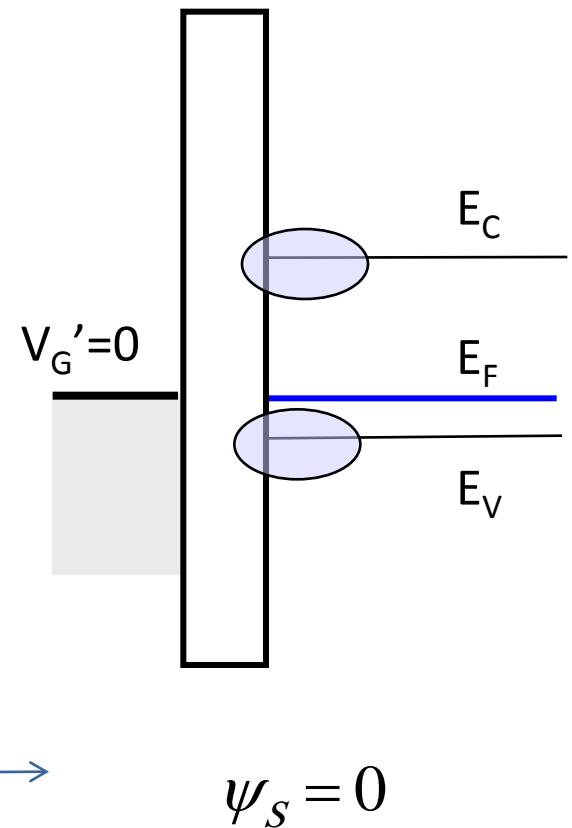
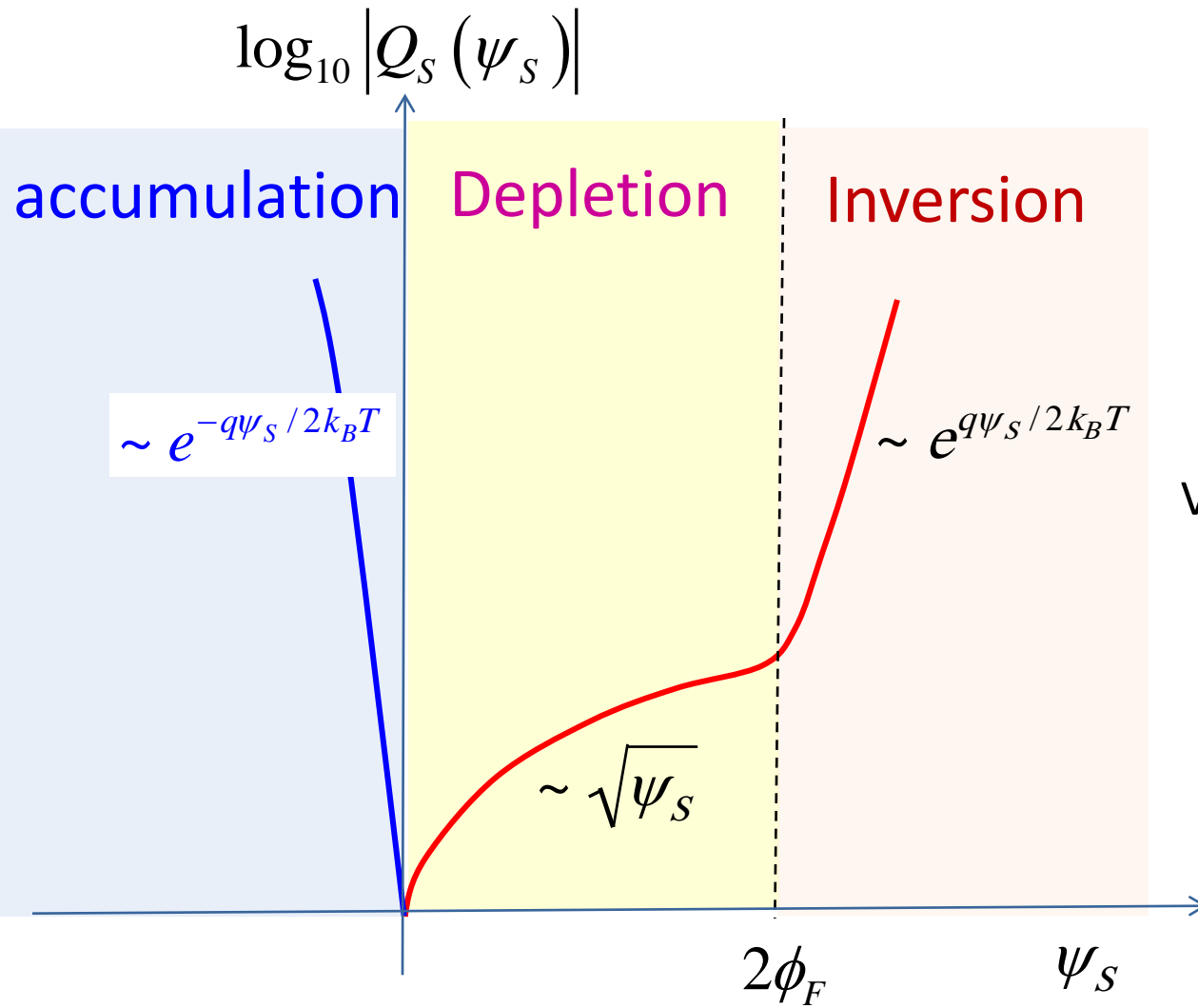
SRH Recombination-Generation

$$R = \frac{np - n_i^2}{\tau_n(p + p_1) + \tau_p(n + n_1)} \rightarrow \frac{-n_i}{\tau_n + \tau_p}$$

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Charges and Surface Potential



Solution of $Q_S(\psi_S)$

$$\nabla \cdot \vec{D} = \rho$$

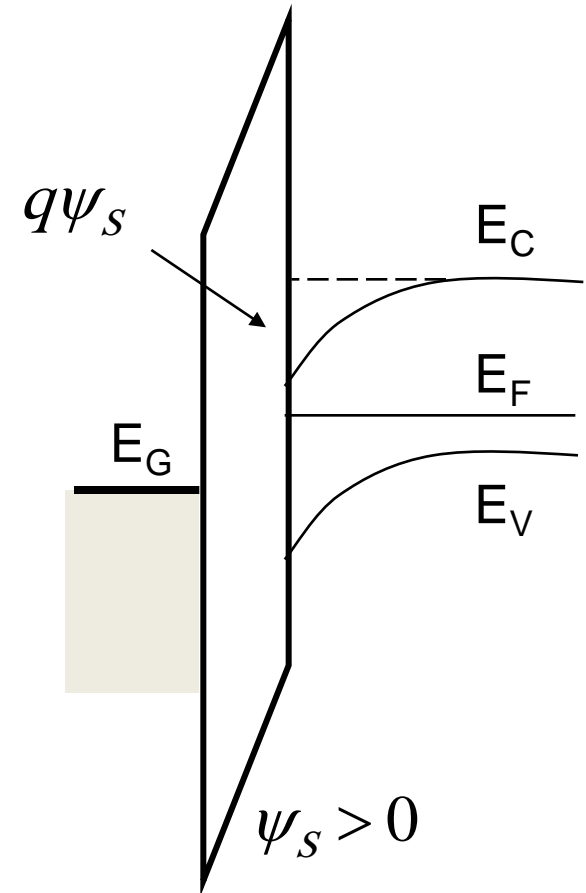
$$\nabla \cdot \left(\vec{J}_n / -q \right) = (G - R)$$

$$\nabla \cdot \left(\vec{J}_p / q \right) = (G - R)$$

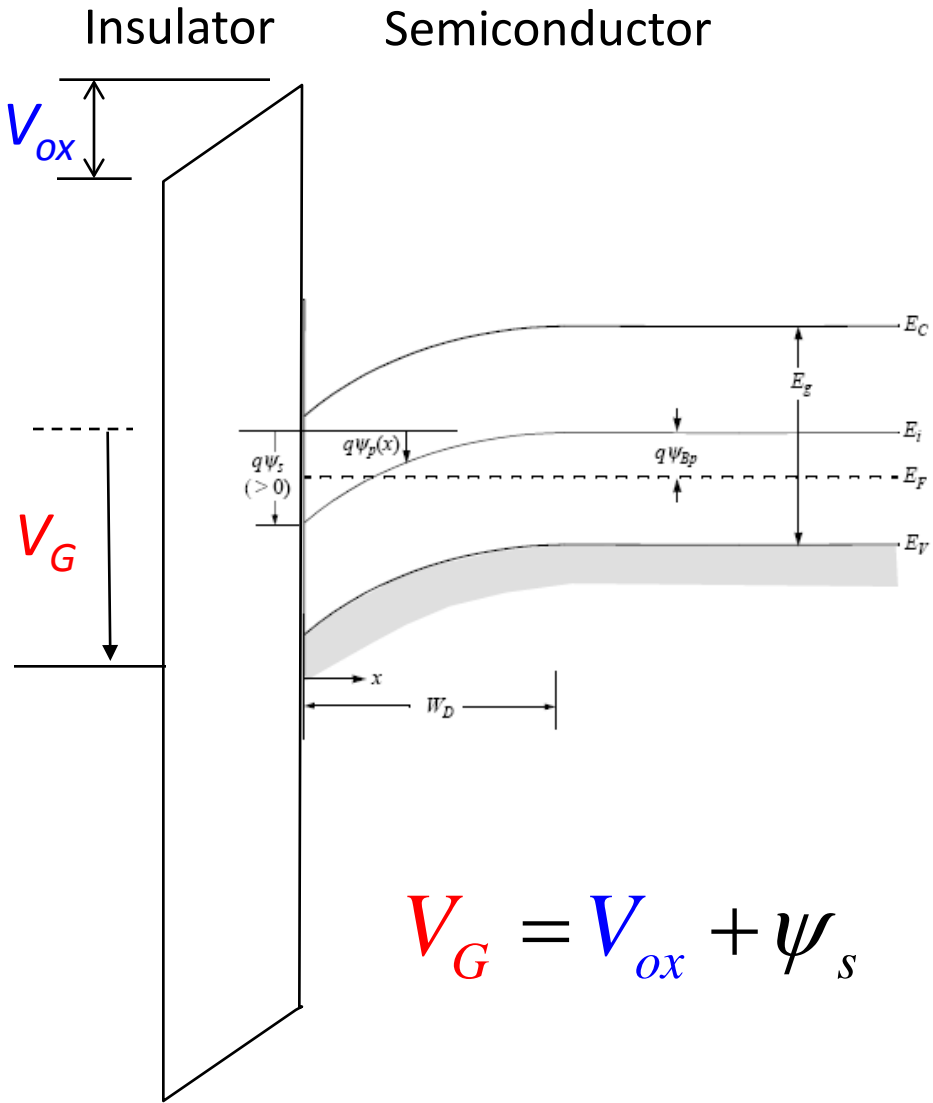
Poisson equation



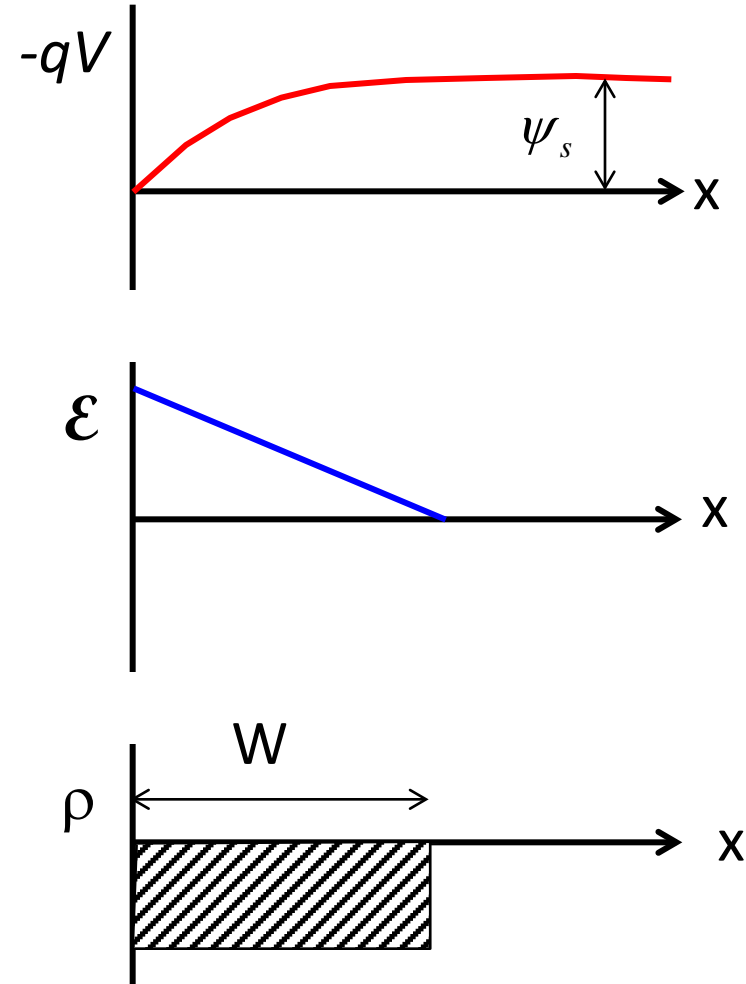
$$\frac{d^2\psi}{dx^2} = \frac{-q}{\kappa_{Si}\epsilon_0} \left[p_0(x) - n_0(x) + N_D^+ - N_A^- \right]$$



(Depletion) Potential, Field, Charges



$$V_G = V_{ox} + \psi_s$$



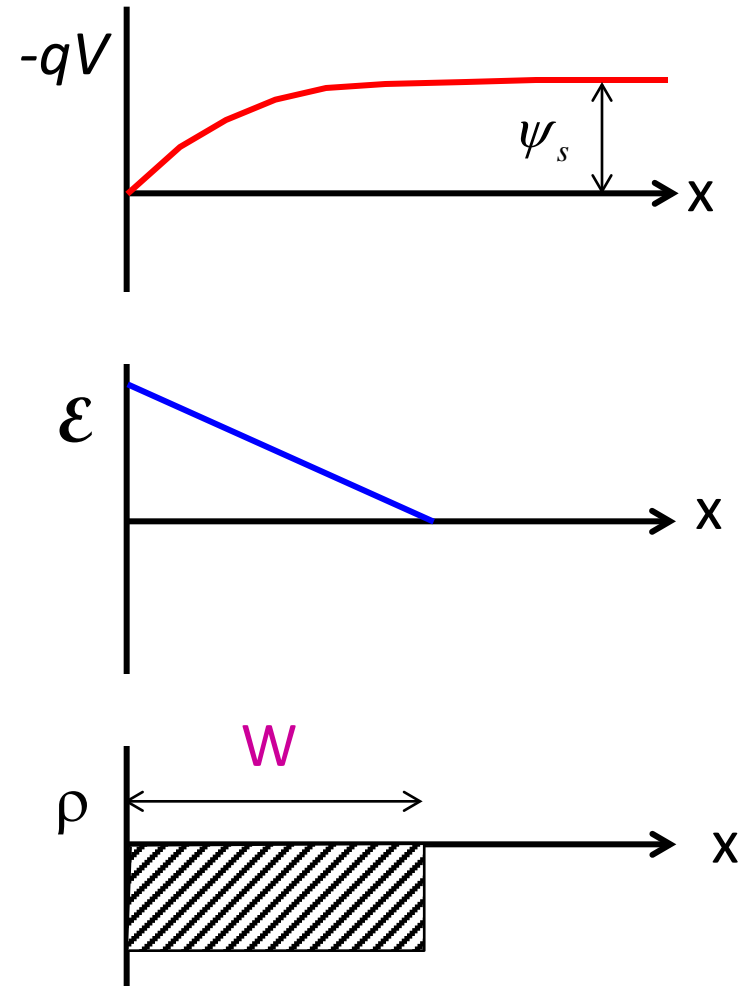
Surface Potential

$$(2) \psi_s = \frac{1}{2} \left(\frac{qN_A W}{\kappa_s \epsilon_0} \right) W = \left(\frac{qN_A W^2}{2\kappa_s \epsilon_0} \right)$$

$$(3) W = \sqrt{\frac{2\kappa_s \epsilon_0 \psi_s}{qN_A}}$$

$$(1) \mathcal{E}(0^+) = -\frac{qN_A W}{\kappa_s \epsilon_0}$$

$$(4) V_G = V_{ox} + \psi_s$$

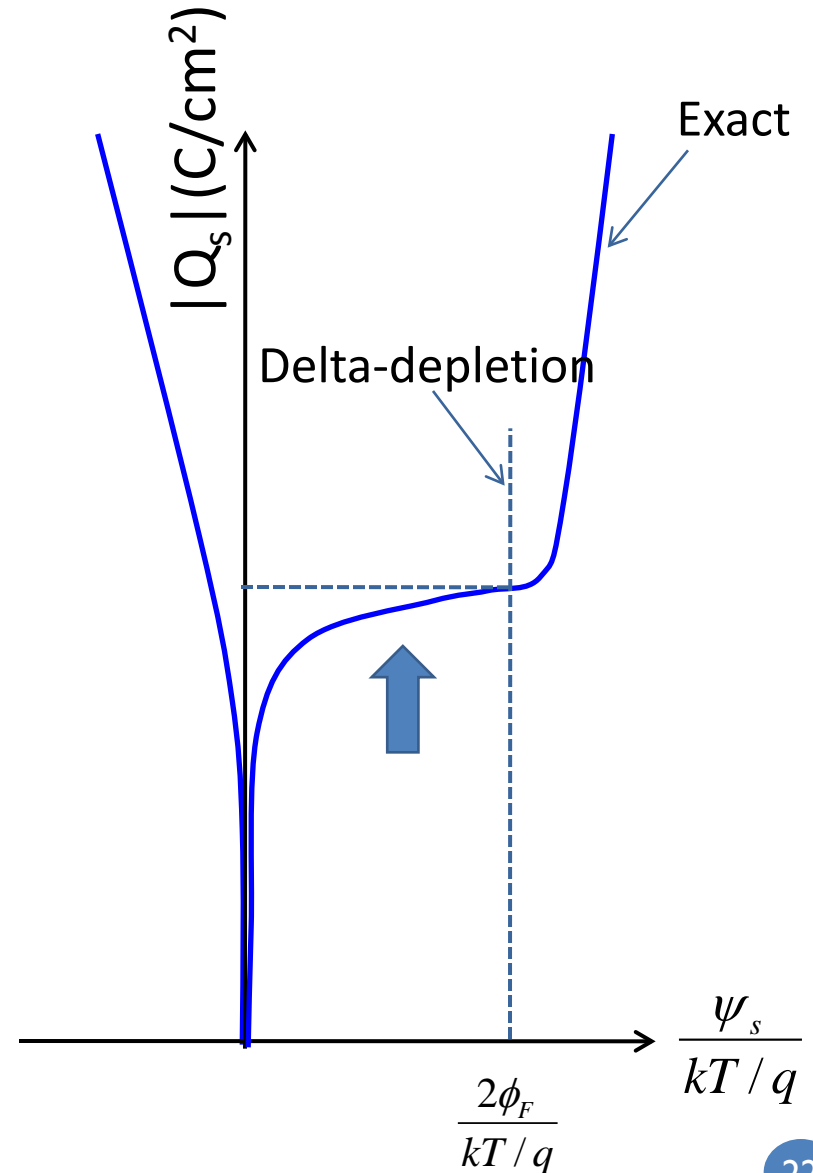


Gate Voltage /Surface Potential in Depletion Region

$$\begin{aligned}
 V_G &= \mathcal{E}_{ox}(0^-) x_0 + \left(\frac{qN_A W^2}{2\kappa_s \epsilon_0} \right) \\
 &= \left[\frac{qN_A W}{\kappa_{ox} \epsilon_0} \right] x_0 + \left(\frac{qN_A W^2}{2\kappa_s \epsilon_0} \right) \\
 &= \frac{qN_A x_0}{\kappa_{ox} \epsilon_0} \sqrt{\frac{2\kappa_{ox} \epsilon_0}{qN_A}} \sqrt{\psi_s} + \psi_s \\
 &\equiv \mathcal{B} \sqrt{\psi_s} + \psi_s
 \end{aligned}$$

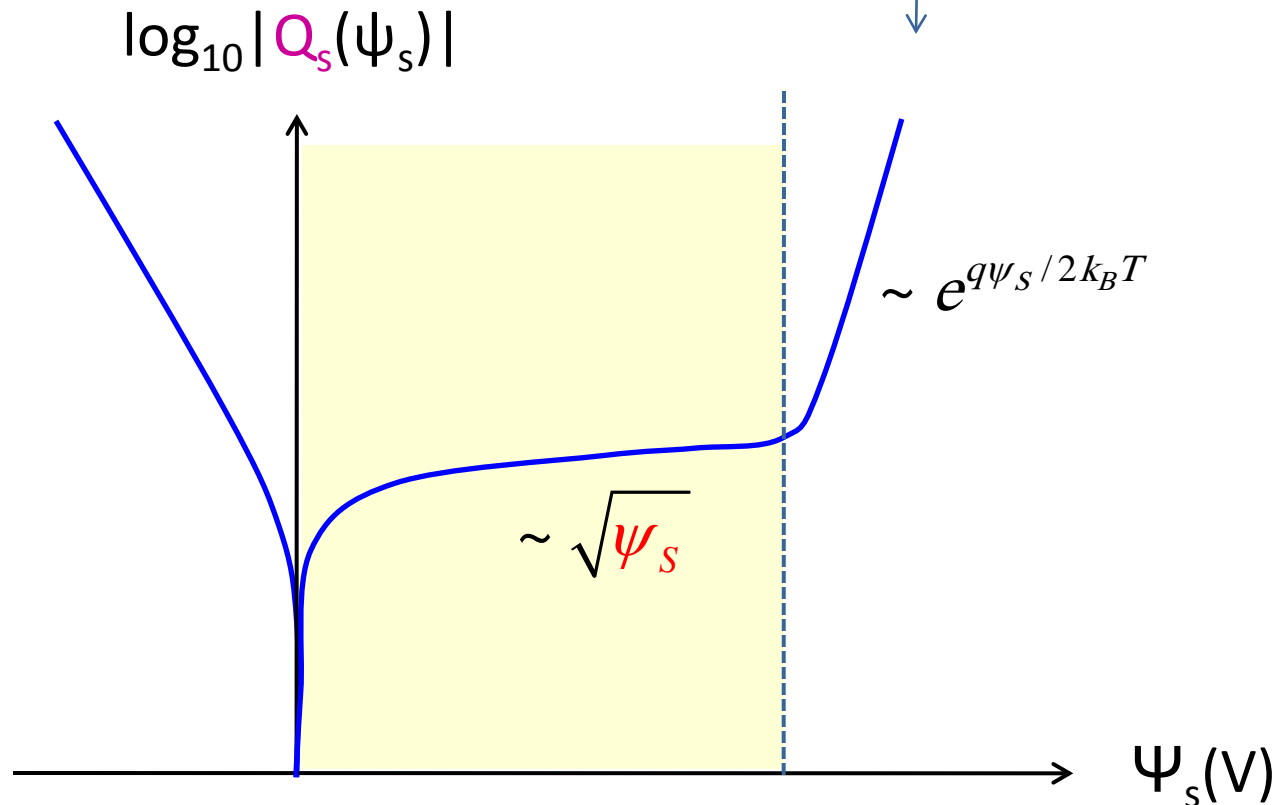
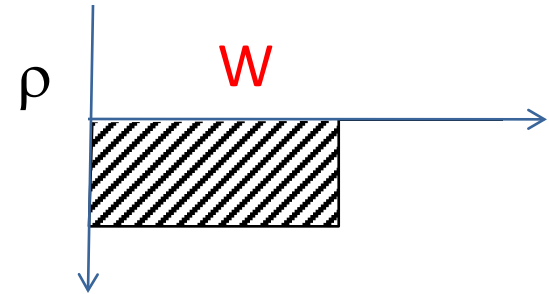
.....because $\psi_s = \left(\frac{qN_A W^2}{2\kappa_s \epsilon_0} \right)$

V_G known, determine ψ_s

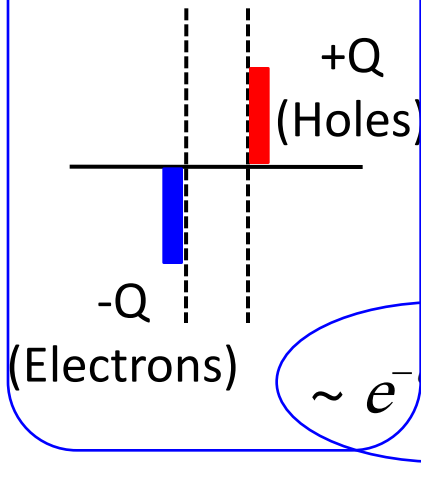
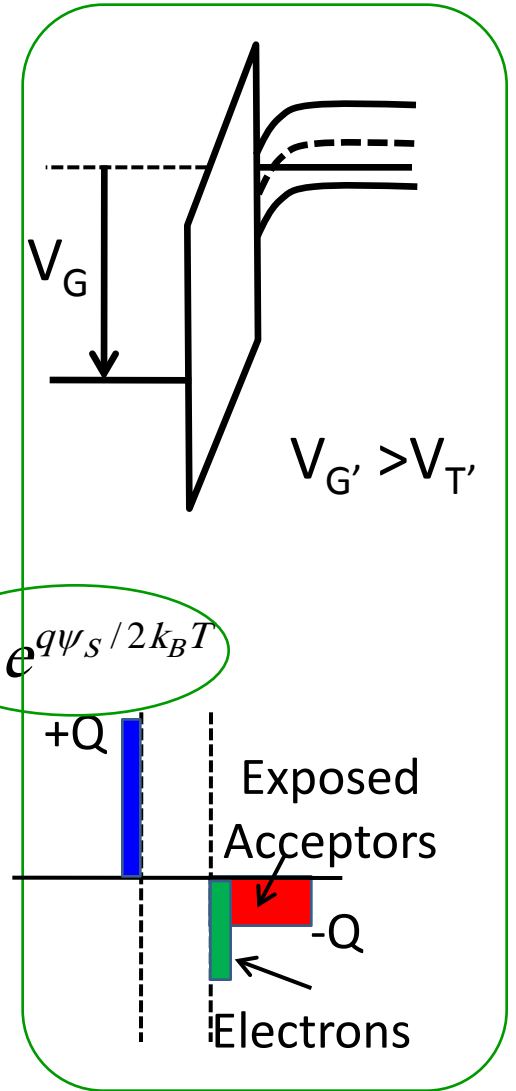
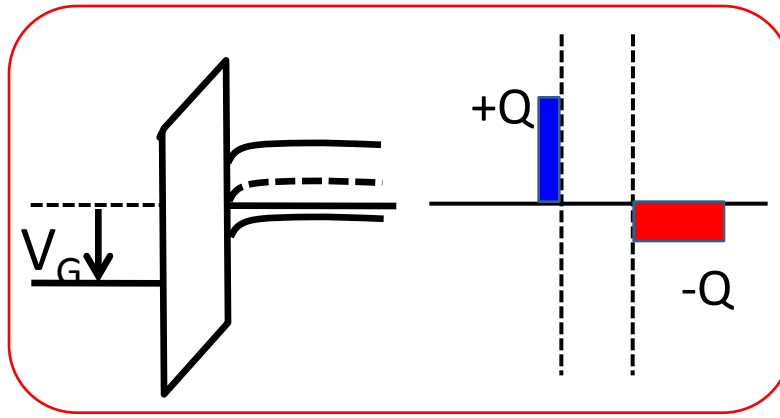
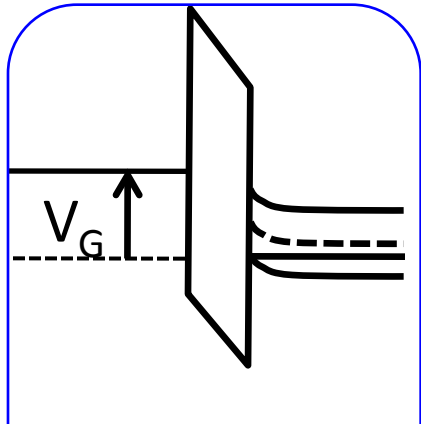


Gate Voltage and Depletion Charge

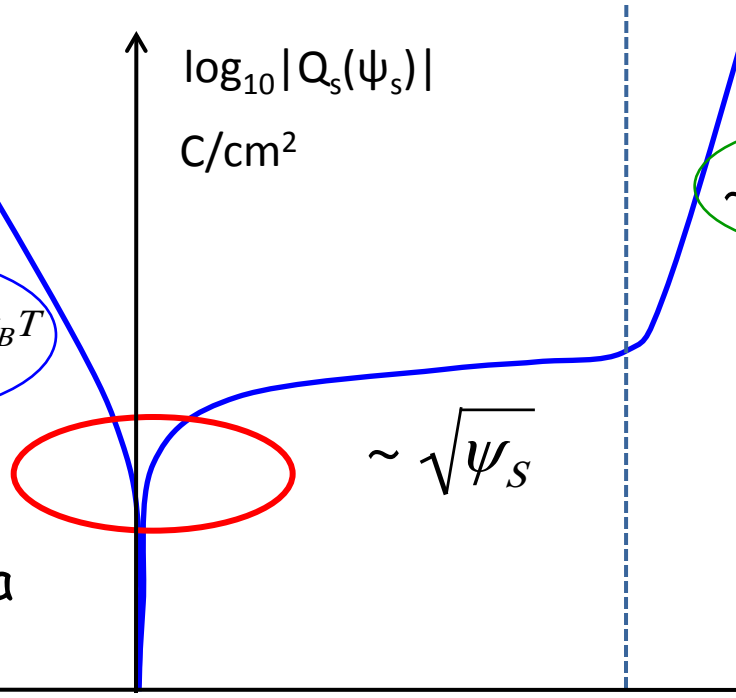
$$Q_s(\psi_s) = -qN_A W = \sqrt{2qN_A \kappa_{Si} \epsilon_0 \psi_s}$$



Surface Potential and Induced Charge



$$\sim e^{-q\psi_s/2k_B T}$$



$$\sim e^{q\psi_s/2k_B T}$$

Why did we not see these phenomena in p-n junctions?

Conclusion

MOSFET is the dominant electronic device now, not because it is superior to BJTs in terms of performance, but because it consumes far less power and allow denser integration.

MOSFET is an inherently 2D device. We separate out the vertical and horizontal components to qualitatively explore the mechanics of its operation.

We explored relation between gate voltage and induced charge for a MOS-C today. We will continue this discussion in the next class.