Essential Physics of Ballistic Nanotransistors:

Exercises with the FETToy Program

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This series of exercises uses the FETToy program available at www.nanohub.org to illustrate some of the key physical concepts for nanotransistors.

Traditional MOSFET models tell us that $I_D \propto C_{ox}$, so reducing the oxide thickness by a factor of two doubles the current. Let's see what happens for nanotransistors.

1) Explore the role of gate oxide thickness on the on-current of a ballistic silicon MOSFET. For these calculations, you should use **1D electrostatics** (gate control parameter = 1 and drain control parameter = 0) and vary the oxide thickness from **10nm** to the unphysically small value of **0.01nm**. Assume V_{DD} = 1V and room temperature operation.

   1a) Produce a plot of the on-current (the current for $V_G = V_D = V_{DD}$) vs. oxide thickness. Compare the computed results to the result expected from conventional MOSFET theory ($I_D \sim C_{OX}$) by appropriately plotting the actual result and the trend expected from traditional theory.

   1b) Provide a physical explanation for the shape of your plot. The characteristic should change when the oxide thickness is smaller than a certain value. Can you give a simple equation to estimate that value? (HINT: It is the gate capacitance that matters. The oxide capacitance is in series with a semiconductor or "quantum" capacitance)

One might think that a lighter effective mass would give a transistor higher current, because with a lighter mass, carriers travel faster. This exercise will demonstrate that this is not always the case.

2) Explore the role of effective mass on the on-current of a ballistic silicon MOSFET. For this calculation, you should also use **1D electrostatics** (gate control parameter = 1 and drain control parameter = 0) and vary the effective mass from $\mathbf{10m_0}$ to $\mathbf{0.01m_0}$. Assume V_{DD} = 1V and room temperature operation.

2a) Produce a plot of the on-current (the current for $V_G = V_D = V_{DD}$) vs. effective mass. You might expect the on-current to be proportional to the velocity (which is inversely proportional to the square root of the effective mass). Compare your plot against this expectation by appropriately plotting the results.

2b) Provide a physical explanation for the shape of your plot. That is, explain why the plot of I_D(on) vs. m^* has a maximum. Hint: consider the influence of the quantum capacitance.

There is considerable interest these days in exploring the use of alternative channel materials such as Ge, GaAs, and InAs. How much performance advantage can be expected from these "new" materials?

3) Compare the on-currents of ballistic silicon, germanium, gallium arsenide, and indium arsenide n-MOSFETs. For this calculation, you should also use **1D electrostatics** (gate control parameter = 1 and drain control parameter = 0) Assume V_{DD} = 1.0V, room temperature operation, and select the appropriate effective mass and valley degeneracies for each case.

3a) Assume an insulator thickness of 5 nm and a dielectric constant of 3.9. Simulate the four ballistic MOSFETs and compare their on-currents.

3b) Assume an insulator thickness of 0.5 nm and a dielectric constant of 3.9. Simulate the four ballistic MOSFETs and compare their on-currents.

3c) Discuss your results and provide a physical explanation for what you observe in the FETToy simulations.

The on-current is commonly used as a device metric, but the entire I-V characteristic is important in a switching transient. How do the shapes of the I_{DS} vs. V_{DS} characteristics of different MOSFETs compare?

4) Simulate ballistic silicon, germanium, gallium arsenide, and indium arsenide n-MOSFETs using an insulator thickness of 1nm. For this calculation, you should also use **1D electrostatics** (gate control parameter = 1 and drain control parameter = 0) Assume V_{DD} = 1V, room temperature operation and select the appropriate effective mass and valley degeneracies for each case. For this exercise, you only need to consider $V_G = V_{DD}$.

4a) Normalize each I_{DS} vs. V_{DS} characteristic by plotting (I_{DS}/I_{ON}) vs. V_G. Plot all four results on the same set of axes and compare the shape.

4b) Discuss your results and provide a physical explanation for any difference that you observe.

"Floating boundary condition" are a complication that we have not emphasized; they are discuss in the paper by Rahman, et al. (*IEEE Trans. Electron. Dev.*, **50**, pp. 1853-1864, 2003).

5) Simulate a ballistic silicon, n-MOSFETs with an insulator thickness of 1nm and V_{DD} = 1V, and room temperature operation. For this calculation, you should also use **1D electrostatics** (gate control parameter = 1 and drain control parameter = 0).

   5a) Compute the transistor characteristics two different ways, with and without the floating boundary condition turned on.

   5a) Normalize each I_{DS} vs. V_{DS} characteristic by plotting (I_{DS}/I_{ON}) vs. V_G. Plot both results on the same set of axes and compare the shape.

   5b) Discuss your results and provide a physical explanation for any difference that you observe in terms of the floating boundary condition physics as discussed by Rahman et al.

A silicon n-MOSFET typically delivers about twice the on-current of a silicon p-MOSFET. This difference is commonly attributed to difference in carrier mobility and saturation velocity. What does a ballistic model predict?

6) Simulate a ballistic silicon, n-MOSFET and a ballistic p-MOSFET using 2nm of SiO_2 for the gate insulator, V_{DD} = 1V, and assuming room temperature operation. For this calculation, you should also use **1D electrostatics** (gate control parameter = 1 and drain control parameter = 0). You will need to identify the appropriate hole effective mass and valley degeneracy.

   6a) Compare the on-currents of the two MOSFETs and explain the difference. Why does the n-MOSFET give higher current?

   6b) Compare the low V_{DS} channel resistances of the two MOSFETs and explain the difference. Is the ratio of the channel resistances the same as the ratio of the on-currents? Provide a physical explanation for the result.

   6c) Repeat parts 6a) and 6b) for a 0.5nm gate insulator.

The temperature dependence of a MOSFET sheds light on its device physics. For a ballistic nanotransistor, we might expect the on-current to decrease at 77K, because the thermal velocity limits it. That is certainly true for the non-degenerate case (where $\upsilon_T \propto \sqrt{T}$), but what happens when the electrons are degenerate, as they typically are above threshold?

7) Explore the role of <u>temperature</u> on the <u>on-current</u> of a ballistic silicon MOSFET. For this calculation, you should also use **1D electrostatics** and vary the <u>temperature</u> from **50K** to **400K**. You should use the ***default*** values for the other parameters.

   7a) Produce a plot of the on-current (the current for $V_G = V_D = V_{DD}$) vs. T. You might expect the on-current to be proportional to the thermal velocity (which is proportional to the square root of the temperature). Compare your plot against this expectation.

   7b) Provide a <u>physical explanation</u> for the shape of your plot.

In FETToy, two-dimensional electrostatics is treated with a simple circuit model and two parameters, a gate control parameter and a drain control parameter.

8) Simulate a ballistic silicon, n-MOSFET using an insulator thickness of 2 nm (SiO_2) and V_{DD} = 1V, and assuming room temperature operation.

   8a) Set the gate control parameter to 1.0 and the drain control parameter to 0.0 and run a simulation. Then examine the plot of charge, Q, vs. V_{GS} at high and low V_{DS}. Explain what determines the slope of the two plots and how you can calculate the slope by hand. Also examine the charge vs. V_{DS} plot and explain why it is not constant.

   8b) Adjust the gate and drain control parameters to give a subthreshold swing of S = 100 mV/decade and a DIBL of 100 mV/V. Repeat the simulation, compare the results to part a) and explain the differences.

   8c) Repeat parts a) and b) but this time use an insulator thickness of 0.5 nm.

Is any of this relevant? Let's see how close to the ballistic limit modern day MOSFETs operate.

9) Review the online seminar, "Performance Analysis of a State-of-the-Art MOSFET," and repeat the analysis for the p-MOS device in the same paper.

Nanowire transistors are getting a lot of attention these days. They seem to operate more nearly as SB FETs than as MOSFETs, but it's interesting so see what might happen if nanowire MOSFETs can be realized. The exercise below will get you calibrated on silicon nanowire MOSFETs.

10) Examine the *I-V* characteristics of a hypothetical silicon nanowire MOSFET. Assume D = 1nm and that the insulator is 2 nm of SiO_2 and that $V_{DD} = 0.5$V. Use an approximate threshold voltage of $V_T = 0.2$V and assume room temperature operation.

10a) Compute I_D vs. V_{DS} at T = 300K and compare the low-V_{DS} drain conductance, G_D with the quantum conductance, $4e^2/h$.

10b) Repeat problem i) but at T = 77K. The channel conductance vs. V_{GS} is strikingly different than a conventional MOSFET. Explain how.

10c) The on-current can be written as $I_D = C_G \langle \upsilon(0) \rangle (V_{GS} - V_T)$. Deduce C_G, $\langle \upsilon(0) \rangle$, and V_T

Both silicon and carbon nanotube nanowire FETs are currently being explored. Let's compare the performance of these two different materials.

11) Compare the performance of a silicon nanowire MOSFET to a carbon nanotube MOSFET as follows:

11a) Simulate a Si nanowire MOSFET with D = 1nm, t_{ins} = 1.5nm, $V_{DD} = 0.5$V, and V_T = -0.2V. Assume SiO_2 as the gate insulator.

11b) Simulate a CNT MOSFET with D = 1nm, tins = 0.5 nm, $V_{DD} = 0.5$V, and V_T = -0.2V. Assume SiO_2 as the gate insulator.

11c) Compare the performance of the two nanowire transistors and explain what the key differences are and why they occur.

One of the potential advantages of carbon nanotubes is that they have no dangling bonds, so it should be easy to deposit high-k gate dielectrics on them. In the next exercise, you will examine carbon nanotube FETs with high-k gate dielectrics.

12) Compare the performance of a D = 1 nm carbon nanotube MOSFET with $\kappa = 3.9$ ($Si0_2$), $\kappa = 15$ (HfO_2) and $\kappa = 25$ (ZrO) and with $\kappa = 80$ (salt water). Plot I_D(on) vs. κ. Explain why the benefits of high-κ gate dielectrics diminish at high κ.

It is possible for ballistic nanowire MOSFETs to operate in a regime where conventional MOSFET theory breaks down. For example, nanotubes have been gated in salt water (k = 80). In this case, the insulator capacitance is much higher that the semiconductor (or quantum capacitance), so that the gate capacitance (the series combination of the two) is simply the quantum capacitance of the nanotube. How does this affect a carbon nanotube MOSFET?

13) Explore the behavior of a carbon nanotube MOSFET in the quantum capacitance limit.

    13a) Simulate a CNT MOSFET with D = 1nm, t_{ins} = 1.5nm, and $\kappa = 80$. Set V_T = -0.2V and assume V_{DD} = 0.5V.

    13b) Compare the channel conductance, $\partial I_D / \partial V_{DS}\big|_{V_{GS}}$ at low drain bias to the transconductance, $\partial I_D / \partial V_{DS}\big|_{V_{GS}}$ at high drain bias. In the quantum capacitance limit, the two are related. <u>Explain</u> why.

Are nanowire MOSFETs inherently superior to conventional MOSFETs with 2D channels?

12) Compare the performance of a hypothetical ballistic Si nanowire MOSFET to that of a planar ballistic MOSFET. Assume t_{ins} = 1.5 nm of SiO_2 in both cases, V_{DD} = 1.0V, and room temperature. For the nanowire, assume D = 1nm. You should assume ideal 1D electrostatics (gate control parameter = 1.0 and drain control parameter = -0.0). To begin, assume V_T = 0.25V for the planar MOSFET. Then use the g_m/I_D vs. V_G plots to adjust the nanowire V_T to match the turn on characteristic of the MOSFET.

12a) Plot I_D/I_D(on) vs. V_{DS} for V_{GS} = 1.0V for the two transistor to compare the shape of the I-V characteristic of the two transistors. Discuss any differences you observe.

12b) Read the following paper to learn how to construct a plot of intrinsic device delay vs. ION/IOFF.

Jing Guo, Hongjie Dai, and Mark Lundstrom, "Performance Analysis and Design Optimization of Near-Ballistic Carbon Nanotube Field-Effect Transistors," presented at the Intern. Electron Devices Meeting, San Francisco, CA, Dec. 2004.

Plot intrinsic device delay for the planar and nanowire MOSFET. Which device is fundamentally the better MOSFET?