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Atomistic Simulations on Reliability

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Abstract: Discrete impurity effects in terms of their statistical variations in number and position in the inversion and depletion region of a MOSFET, as the gate length is aggressively scaled, have recently been researched as a major cause of reliability degradation observed in intra-die and die-to-die threshold voltage variation on the same chip resulting in significant variation in saturation drive (on) current and transconductance degradation –two key metrics for benchmark performance of digital and analog integrated circuits. In the following chapter, the authors have highlighted the random dopant fluctuation (RDF) based Ensemble Monte Carlo (EMC) device simulation study conducted by the Computational Electronics (COMPUTEL) research group of Arizona State University. In addition to RDF, random number and position of interface traps lying close to Si:SiO_2 interface engender additional concerns leading to enhanced experimentally observed fluctuations in drain current and threshold voltage. In this context, the authors of this chapter present novel EMC based simulation studies on trap induced random telegraph noise (RTN) responsible for statistical fluctuation pattern observed in threshold voltage, its standard deviation and drive current in saturation for 45 nm gate length MOSFET device. From the observed simulation results and their analysis, it can be cogently projected that with continued scaling in gate length and width, RTN effect will eventually supersede as a major reliability bottleneck over the typical RDF phenomenon. The fluctuation patterns observed by EMC simulation outcomes for both drain current and threshold voltage have been analyzed and explained from analytical device physics perspectives.

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1. Introduction

The transistor mismatch due to random variations in process parameters has become one of the major issues in deep-submicrometer technology. The term transistor mismatch refers to the fact that supposedly identical transistors at the design phase come out as distinct devices after manufacturing due to process variations. The extrinsic factors include variation in the implantation dose and energy, oxidation and annealing temperatures, etc. On the other hand, the intrinsic factors include variations due to channel dopant number, interface, and fixed oxide charge. Both the extrinsic and the intrinsic factors influence the transistor output performance and yield. The transistor mismatch effect will become worse in the future due to demanding requirement on process tolerance. Hence, there is a direct need to develop a very good understanding on the impact of variation in a given unit process on resulting variation in a given circuit parameter. This will enable the process engineering and manufacturing team to define appropriate process monitor and control criteria for all the unit processes involved. This will also help during the technology development phase to select a particular process integration scheme that could minimize the mismatch among various available options. In this book chapter we first discuss the impact of discrete impurity effects on critical device parameters (Section 2). In Section 3 we elaborate on the influence of the random telegraph noise fluctuations on the variation in the threshold voltage and device on current. Conclusions from this work are presented in Section 4.

2. Discrete Impurity Effects

2.1 Some General Considerations

Statistical fluctuations of the channel dopant number were predicted by Keyes [13] as a fundamental physical limitation of MOSFETs down-scaling. Entering into the nanometer regime results in a decreasing number of channel impurities whose random distribution leads to significant fluctuations of the threshold voltage and off-state leakage current. These effects are likely to induce serious problems on the operation and performances of logical and analog circuits.

It has been experimentally verified by Mizuno and co-workers [17] that threshold voltage fluctuations are mainly caused by random fluctuations of the number of dopant atoms (RDF) and other contributions such as fluctuations of the oxide thickness are comparably very small. It follows from these remarks that impurities cannot be considered anymore using the continuum doping model in advanced semiconductor device modeling but the precise location of each individual impurity within a full Coulomb interaction picture must be taken into account.

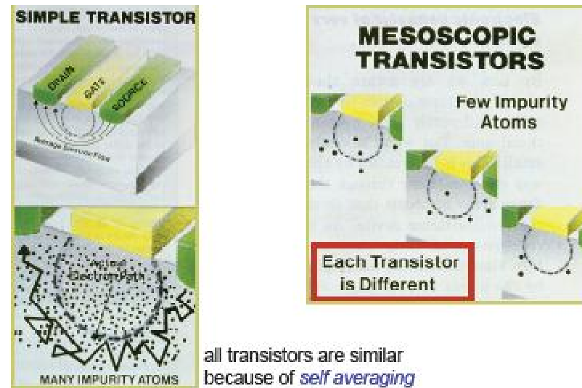

Fig. 1. The role of discrete impurities in large devices (left panel) and in mesoscopic devices (right panel).

2.2 *Drift-Diffusion Simulations of Discrete Impurity Effects*

To illustrate the importance of the discrete impurity effects on the threshold voltage and the off-state current, in 1996 the group from ASU simulated a number of MOSFET device structures [20]. The corresponding potential profile under equilibrium conditions along the depth and in the plane parallel to the semiconductor/oxide interface is shown in the top and bottom panels of Fig. 2. In our analysis we have found that it is not only the total number of atoms within the discrete doping region that matters, but the location of these atoms plays very important role.

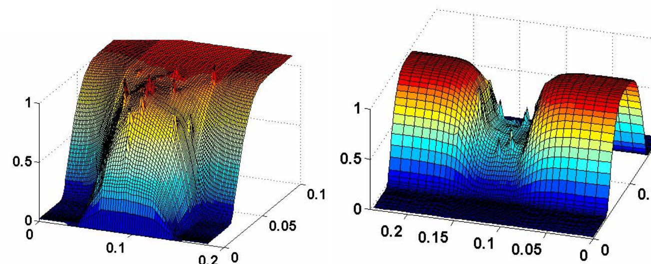

Fig. 2. Top panel: potential profile in a cut through the depth of the device. Bottom panel: potential profile in the semiconductor in a plane parallel to the semiconductor/oxide interface.

Illustrated in Fig. 3, are the potential profiles and the current stream lines for two impurity distributions. Note that the significant current crowding in the upper panel near the critical source end of the channel leads to smaller drain current for

V_D = 50 mV and a range of V_G values. This, in turn, results in larger threshold voltage for this device.

With the down-scaling of MOSFET devices, electrons in the conducting channel are in ever closer proximity to the high-density electron gases present in the source and drain regions—separated from each other by as little as tens of nanometers—and in the polycrystalline Si gate—separated from the channel by as little as 1.5 nm of SiO_2. As studied in [6], the role of these long-range Coulomb interactions is two-fold: (1) The interaction between electrons in the channel and the high-density electron gases in the source and drain regions can be pictured classically as a reshaping of the electron distribution in the channel caused by the potential-fluctuations, associated with plasma oscillations in the source and drain regions, leaking into the low-density channel. Quantum-mechanically, this corresponds to emission and absorption of plasmons by the channel electrons. While these processes do not subtract directly momentum from the electron gas, their net effect is a thermalization of the hot electrons energy distribution in the channel, the resulting higher energy tail being affected by additional momentum-relaxation processes (phonons, ionized impurities). This causes, indirectly, a reduction of the effective electron velocity in the channel, and so, a depression of the transconductance as the channel length is reduced below about 4 nm. On the other hand, the interaction between channel-electrons and electrons in the gate (Coulomb drag across the very thin insulator) results in a direct loss of momentum of the electrons in the channel. Semi-classically, this interaction—also plasmon-mediated—has been studied by a group at IBM [7] predicting a significant depression of the electron velocity for SiO_2 layers thinner than about 2–3 nm. This behavior has also been observed experimentally [15], recent results being in quantitative agreement with early theoretical estimates.

2.3 Monte Carlo Device Simulations of Discrete Impurity Effects

In the past, the effect of discrete dopant random distribution in MOSFET channel has been assessed by analytical or drift-diffusion (DD) approaches. The first DD study consisted in using a stochastically fluctuating dopant distribution obeying Poisson statistics [21]. 3D atomistic simulators have also been developed for studying threshold voltage fluctuations [10, 2] Even though the DD/HD (hydrodynamic) methods are very useful because of their simplicity and fast computing times, it is not at all clear whether such macroscopic simulation schemes can be exploited into the atomistic regime. In fact, it is not at all clear how such discrete electrons and impurities are modeled in macroscopic device simulations due to the long-range nature of the Coulomb potential. 3D DD/HD macroscopic models may be accurate for modeling the threshold voltage fluctuations (since the device is in the off-state) but they are definitely not accurate when examining the on-state current fluctuations.

Three-dimensional Monte Carlo (MC) simulations should provide a more realistic transport description in ultra-short MOSFETs, in particular in the on-state.

The MC procedure gives an exact solution of the Boltzmann transport equation. It, thus, correctly describes the non-stationary transport conditions. Even if microscopic simulations such as the MC method are concerned, the treatment of the electrons and impurities is not straightforward due to, again, the long-range nature of the Coulomb potential. The incorporation of the long-range Coulomb potential in the MC method has been a long-standing issue [18]. This problem is, in general, avoided by assuming that the electrons and the impurities are always screened by the other carriers so that the long-range part of the Coulomb interaction is effectively suppressed. The complexity of the MC simulation increases as one takes into account more complicated screening processes by using the dynamical and wave-vector dependent dielectric function obtained from, for example, the random phase approximation. Indeed, screening is a very complicated many-body matter [5].

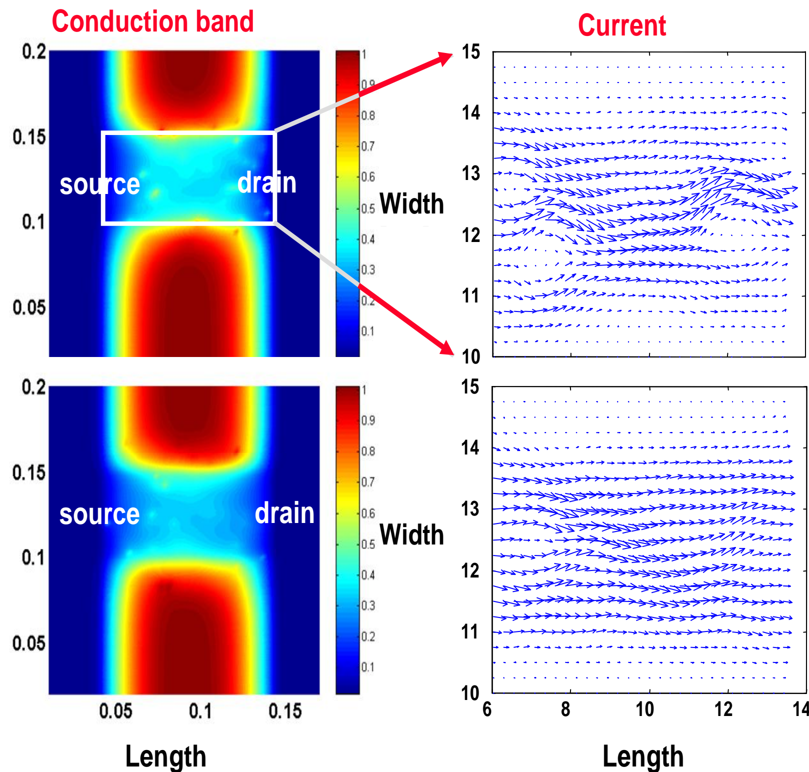

Fig. 3. Potential profile and current stream lines in a 50 nm gate-length MOSFET device. Shown here are two impurity distributions in the device active region.

A novel approach has been introduced by the ASU group [11], in which the MC method is supplemented by a *molecular dynamics* (MD) routine. In this approach, the mutual Coulomb interaction among electrons and impurities is treated in the drift part of the MC transport kernel. Indeed, the various aspects associated with the Coulomb interaction, such as dynamical screening and multiple scatterings, are automatically taken into account. Very recently, the MC/MD method has been extended for spatially inhomogeneous systems. Since a part of the Coulomb interaction is already taken into account by the solution of the Poisson equation, the MD treatment of the Coulomb interaction is restricted only to the limited area near the charged particles. It is claimed that the full incorporation of the Coulomb interaction is indispensable to reproduce the correct electron mobility in highly doped silicon samples.

Although real space treatments eliminate the problem of double counting of the force, a drawback is that the 3D Poisson equation must be solved repeatedly to properly describe the self-consistent fields which consume over 80% of the total simulation time. To further speed up simulations, the ASU team has, for the first time, utilized a 3D Fast Multi-pole Method (FMM) [9, 3, 4, 8] instead. The FMM allows calculation of the field and the potential in a system of n particles connected by a central force within $O(n)$ operations given certain prescribed accuracy. The FMM is based on the idea of condensing the information of the potential generated by point sources in truncated series expansions. After calculating suitable expansions, the long range part of the potential is obtained by evaluating the truncated series at the point in question and the short range part is calculated by direct summation. The field due to the applied boundary biases is obtained at the beginning of the simulation by solving the Laplace equation. Hence the total field acting on each electron is the sum of this constant field and the contribution from the electron-electron and electron-impurity interactions handled by the FMM calculations. The image charges, which arise because of the dielectric discontinuity, are handled by the method of images [14].

Next we present several success stories on the use of our 3D particle-based device simulation code that properly takes into account the short range and the long range Coulomb forces (Fig. 4). We begin with the example of energy relaxation of the carriers at the drain end of the MOSFET channel. The simulated device has channel length L_G = 80 nm, channel width W_G = 80 nm and oxide thickness T_{ox}=3 nm. The lateral extension of the source and drain regions is 50 nm. The channel doping equals 3×10^{18} cm^{-3}. The applied bias is $V_G = V_D = 1$ V. Only those electrons that entered the channel region from the source side were "tagged" and their energy and position was monitored and used in the average energy calculation. From the average velocity simulation results, it follows that the short-range electron-electron (*e-e*) and electron-impurity (*e-i*) interaction terms damp the velocity overshoot effect, thus increasing the transit time of the carriers through the device; thus reducing its cut-off frequency. It is also quite clear that when we use the mesh force only, i.e. we skip the MD loop that allows us to correct for the short-range *e-e* and *e-i* interactions, those electrons that enter the drain end of the device from the channel never reach equilibrium. Their average energy is more

than 60 meV far into the drain region. Also, the average energy peaks past the drain junction. The addition of the short-range Coulomb forces to the mesh force via the MD loop, leads to rapid thermalization of the carriers once they enter the drain region. The characteristic distance over which carriers thermalize is on the order of a few nm.

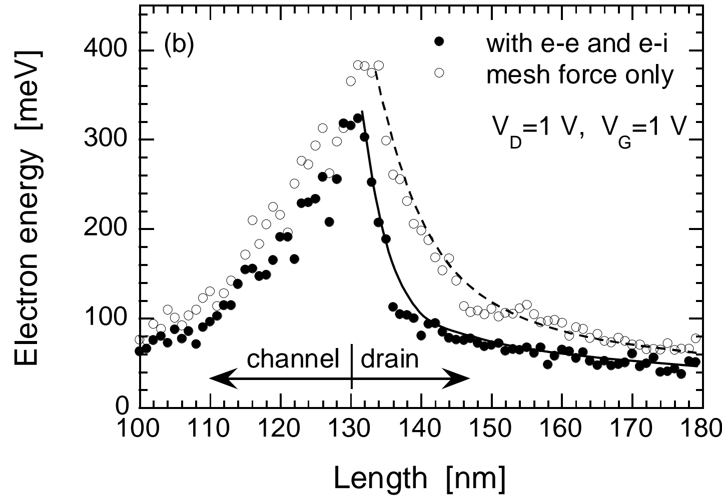

Fig. 4. Average energy of the electrons coming to the drain from the channel. The applied bias equals $V_D = V_G = 1$ V. Filled (open) circles correspond to the case when the short-range *e-e* and *e-i* interactions are included (omitted) in the simulations.

Second important example we have chosen in this paper is the quantitative prediction of the threshold voltage fluctuations versus device gate width, channel doping and oxide thickness, that are shown in Fig. 5. Also shown in this figure are the analytical model predictions derived from experimental studies by Mizuno, Okamura, and Toriumi [17], according to which

$$\sigma_{vt} = \left(\frac{\sqrt[4]{q^3 \varepsilon_s \phi_b}}{\sqrt{2}\varepsilon_{ox}} \right) \frac{T_{ox} \sqrt[4]{N}}{\sqrt{L_{eff} W_{eff}}} \ , \qquad (1)$$

where N is the average channel doping density, ϕ_b is the built-in potential, T_{ox} is the oxide thickness, L_{eff} and W_{eff} are the effective channel length and width, and ε_s and ε_{ox} are the semiconductor and oxide permittivity, respectively. Stolk, Widdershoven and Klaassen [19] generalized the analytical result by Mizuno and his co-workers, by taking into account the finite thickness of the inversion layer, depth-distribution of charges in the depletion layer and the influence of the source

and drain dopant distributions and depletion regions. For a uniform channel dopant distribution, the analytical expression for the threshold voltage standard deviation simplifies to

$$\sigma_{vt} = \left(\frac{\sqrt[4]{q^3 \varepsilon_s \phi_b}}{\sqrt{3}} \right) \left[\frac{k_b T}{q} \cdot \frac{1}{\sqrt{4 \varepsilon_s \phi_b N_a}} + \frac{T_{ox}}{\varepsilon_{ox}} \right] \frac{\sqrt[4]{N}}{\sqrt{L_{eff} W_{eff}}} . \tag{2}$$

In Eq. (2), the first term in the square brackets represents the surface potential fluctuations whereas the second term represents the fluctuations in the electric field. The decrease of the threshold voltage fluctuations with increasing the width of the gate is due to the averaging effects, in agreement with the experimental findings by Horstmann *et al.* [12]. We want to point out that we still observed significant spread of the device transfer characteristics along the gate voltage axis even for devices with $W_G = 100$ nm. This is due to the nonuniformity of the potential barrier, which allows for early turn-on of some parts of the channel. As expected, the increase in the channel doping leads to larger threshold voltage standard deviation $\sigma_{V_{TH}}$. These results also imply that the fluctuations in the threshold voltage can be even larger in devices in which counter ion implantation is used for threshold voltage adjustments. Similarly, the increase in the oxide thickness leads to linear increase in the threshold voltage standard deviation. The results shown in Fig. 5(a-c) also suggest that reconstruction of the established scaling laws is needed to reduce the fluctuations in the threshold voltage. In other words, within some new scaling methodology, T_{ox} should become much thinner, or N_A much lower that what the conventional scaling laws give.

To further elaborate on the role of Coulomb interactions, in Example 3, as suggested by the results presented in Example 2, we consider 50 nm channel length narrow-width SOI device with undoped channel. The results presented in Fig. 6 also suggest that there are fluctuations in the device threshold voltage for devices fabricated on the same chip due to unintentional doping and random positioning of the impurity atoms. This can also be deduced from the scatter of the experimental data from [16]. The simulation results of the transfer characteristics with a single impurity present in different regions in the channel of the device, shown in the top panel of Fig. 6, clearly demonstrate the origin of the threshold voltage shifts for devices with 10 nm and 5 nm channel width. The width dependence of the threshold voltage for the case of a uniform (undoped) and a discrete impurity model is shown in the bottom panel of Fig. 6. These results suggest that *both size-quantization effects and unintentional doping must be concurrently considered to explain threshold voltage variation in small devises.*

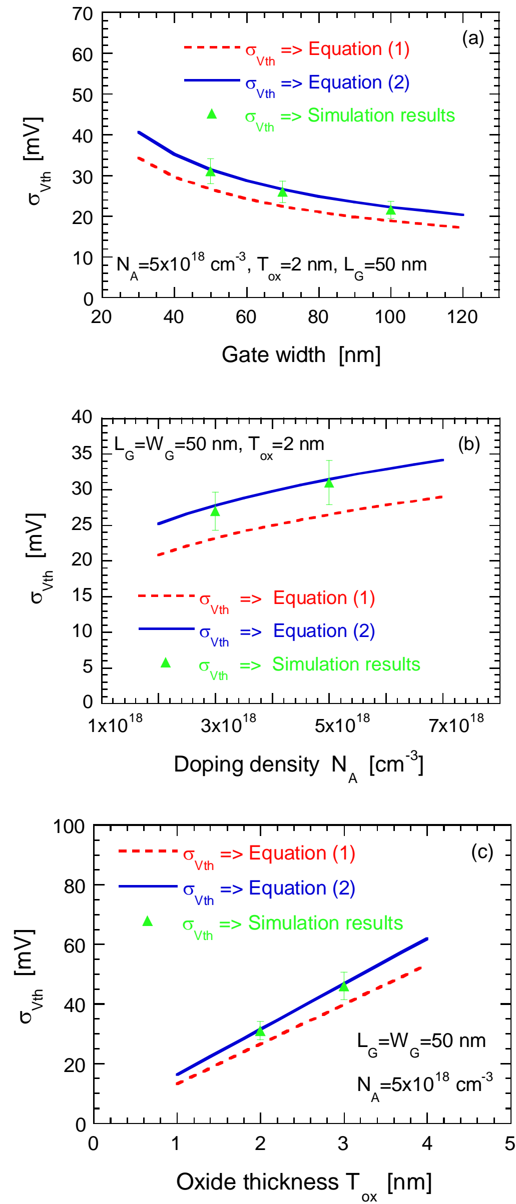

Fig. 5. Variation of the threshold voltage with (a) gate width, (b) channel doping, and (c) oxide thickness.

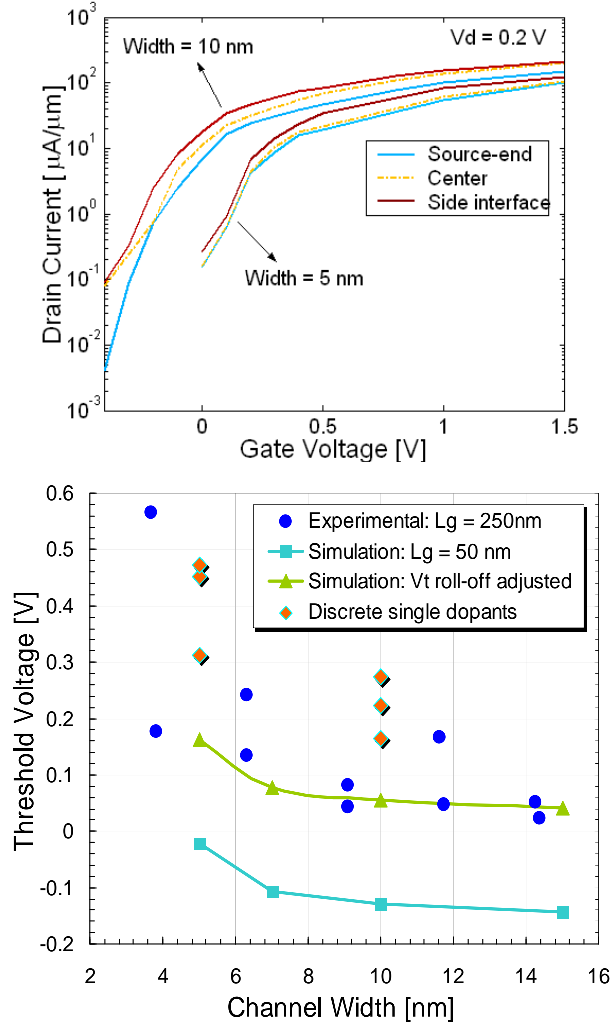

Fig. 6. Top Panel: Transfer characteristics of the device with 10 nm and 5 nm channel widths and different location of the impurity atoms. Bottom Panel: Width dependence of the threshold voltage for the case of a uniform and a discrete impurity model. Clearly seen in this figure are two trends: (a) Threshold voltage increase with decreasing channel width due to quantum-mechanical size quantization effects, and (b) Scatter in the threshold voltage data due to unintentional doping.

3. Random Telegraph Signal

3.1 Importance of Random Trap Fluctuations

The single most important interface in semiconductor technology is that between silicon and its thermally grown oxide. This interface with its propensity to surface micro-roughness after in-situ fabrication plays a crucial role in the performance of today's high speed MOSFET devices. The degree of perfection of the interface has been stipulated to be really exacting in terms of process integrity where a typical device-quality interface has defect densities on the interfacial plane of the order of 10^8-10^{10} cm^{-2} eV^{-1} resulting in defect densities of the order of 1 to 100 defects per square micron assuming the defects are located within one eV of energy distribution from the Fermi energy. As the device area is shrunk to aggressively scaled sub-μm^2 size with scaling-preserved process tolerances, the number of defect densities do show an upward trend and considering that 10^{11} cm^{-2} eV^{-1} values are at least readily encountered, the number of defects seem to reduce to less than 3 in number per square micron within an eV energy distribution for a device size of W×L = 50 nm × 50 nm. The reason reliability concern did not arise in wide gate area technology generation is because with a good number of traps lying within a few eV of Fermi energy, the spatial distribution of energy levels is more tighter making the energy barrier values ΔE_B a fraction of an eV. Hence the carriers trapped in traps easily reemit to inversion layers making RTS amplitude variation almost nonexistent. But in today's aggressively scaled device size, even though the trap numbers are countable and sparse, these traps can be located deep within the oxide with higher ΔE_B differential and a carrier once trapped in a trapped site, may stay there for a prolonged period of time and never get re-emitted to inversion layer causing severe RTS amplitude drawbacks. The surface level trap lying close to the interface can block the carrier flow in the channel by causing local potential fluctuations where significant spread of RTS variation can be observed for even a single trap closer to source side to mid-channel zone impeding the carrier flow. Also one way carrier gets trapped and get detrapped is through tunneling from inversion layer to a trap location and in earlier technological generation with thicker gate oxide, tunneling was not as significant as it is today with the gate-oxide reaching nanometric thickness. The conclusion is with the channel electrons being random, presence of very few defects will suffice to cause notable RTS related device operation failure for current ongoing technological generation of MOSFETs,

Fig. 7(top panel) illustrates the measurement data from a 90nm SRAM design [1]. The minimum supply voltage (V_{ccmin}), which is highly sensitive to device threshold voltage, exhibits a similar pattern in the time domain as that of RTF. The impact of RTF in this case is more than 200mV, which is catastrophic to the yield and low-power design of SRAM. Therefore, accurate and physical models of RTF are essential to predict and optimize circuit performance during the design stage. Currently, such models are not available for circuit simulation. The compound between RTF and other sources of variation, such as RDF, further compli-

cates the situation especially in extremely scaled CMOS design. Fig. 7(bottom panel) shows a typical two level RTS signal time domain characteristics.

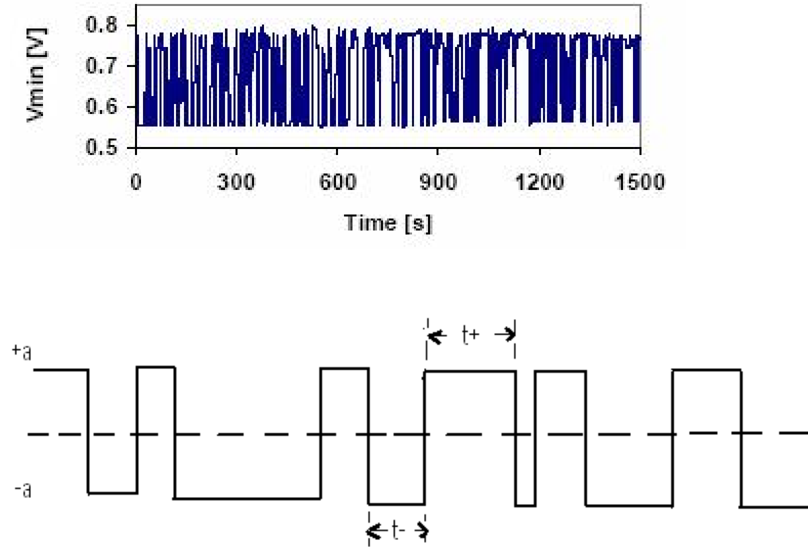

Fig. 7. Top panel: The fluctuation of SRAM V_{ccmin} due to RTF. Bottom panel: A random telegraph signal (namely x(t)) produced by a carrier trap.

3.2 Monte Carlo Device Simulations of Random Traps at the Semiconductor/Oxide Interface

In this research work the integration of random defects positioned across the channel at the Si/SiO_2 interface from source end to the drain end in the presence of different random channel and bulk dopant distributions are used to conduct Ensemble Monte-Carlo (EMC) based numerical simulation of key device performance metrics for 45 nm gate length MOSFET device. The two main performance parameters that affect RTF based reliability measurements are percentage change in relative drain current fluctuation, particularly in the saturation region where most digital circuits operate and percentage change in threshold voltage that affects the device transconductance and on-current drive.

The simulator described in the previous section is presently being used in the investigation of the random trap fluctuations in 45 nm technology node MOSFET

device where, in addition to the randomness of the position and the actual number of the impurity atoms in the whole simulated domain of the device, a random double-charged trap is introduced in the middle section of the channel and moved from the source-end to the drain end of the channel. An example of a discrete impurity pattern and a double trap located at the source-end of the channel is shown in Fig. 8. The effective channel length of 45 nm technology node is taken to be 35 nm.

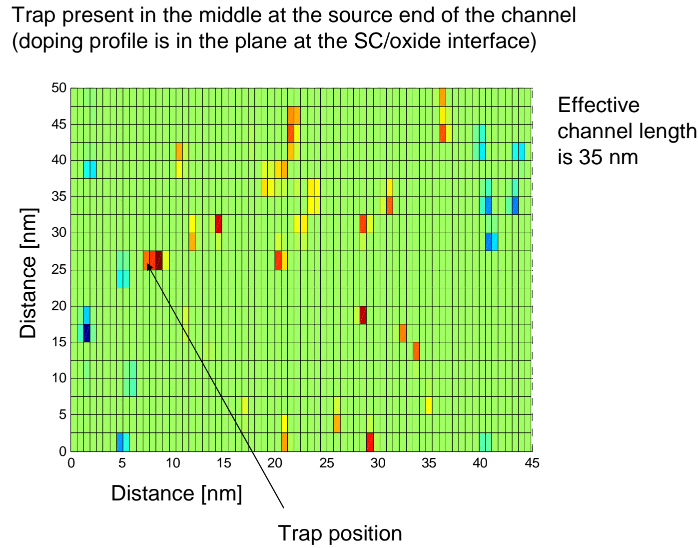

Fig. 8. random dopant distribution and a double trap located in the middle of the source end of the channel.

We consider ensemble of 20 devices with different random dopant distribution. The threshold voltage of each of these 20 devices without the presence of the trap is shown in Fig. 9.

The total variation of the threshold voltage as a function of the double trap position in the middle portion of the channel, when moved from the source end to the drain end of the channel, is shown in Fig. 10. We see that the threshold voltage increases from its average value when the double trap is located at the source end of the channel. This is due to the fact that carriers see additional large potential barrier due to the presence of the charged double trap and are reflected back in the source contact. The threshold voltage reduces when the double trap is moved away from the source injection barrier because when the electrons are injected in the channel, even though the electric field is small (due to small drain bias applied when measuring threshold voltage), they slowly drift towards the drain contact.

In Fig. 11 we depict the threshold voltage standard deviation variation as a function of the double trap position when the double trap is being moved from the

middle of the source end of the channel to the middle of the drain end of the channel. An explanation of the results given in Fig. 11 is schematically shown in Fig. 12. At threshold voltage, the sheet electron density in the channel is small, therefore screening is not important. Traps near the source end of the channel have the largest influence since they are major obstacles to the electrons because of the large input barrier depicted in case (a) shown on the left panel of Fig. 12. Traps near the drain end of the channel have smaller influence since electrons are accelerated by the small electric field – case (b) shown on the right panel of Fig. 12.

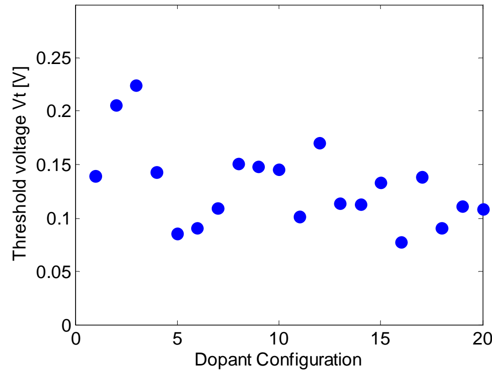

Fig. 9. Threshold voltage fluctuations due to random dopant fluctuations (without traps) for a statistical ensemble of 20 devices with different number and different distribution of the impurity atoms.

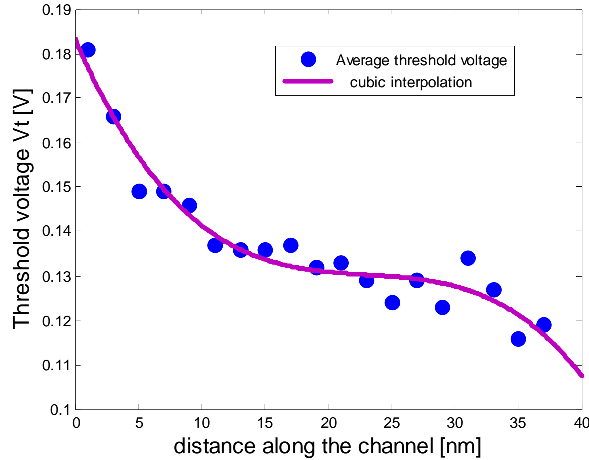

Fig. 10. Threshold voltage variation with trap position variation. These results are averages over the ensemble of 20 devices.

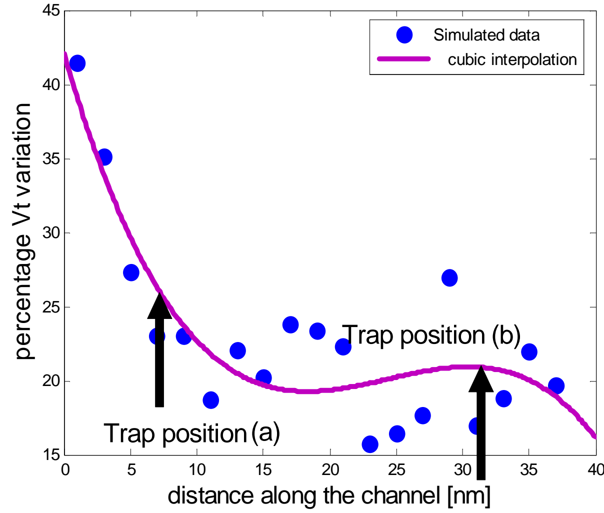

Fig. 11. Percentage threshold voltage fluctuation due to a double trap located at the semiconductor/oxide interface and different position along the middle section of the channel. 20 devices with different random dopant distributions have been averaged out. Detailed description of the trend of the results shown in this figure is given in Figure 12 below.

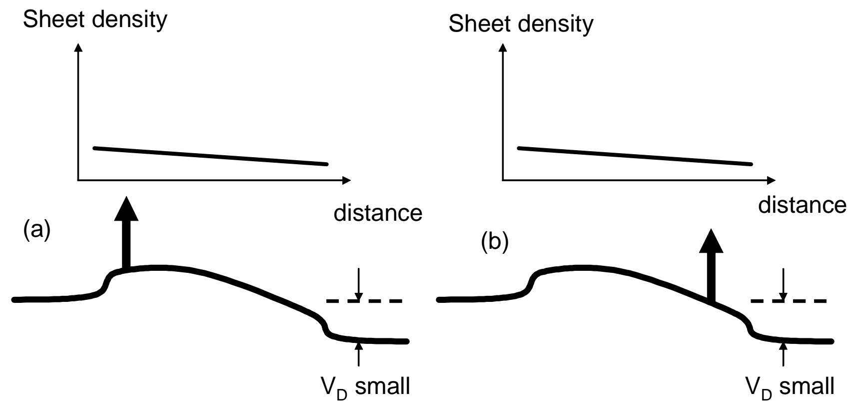

Figure 12. Schematic explanation of the results from Fig. 11.

Fig. 13 shows the ON-current degradation as a function of the double trap position. As depicted on the figure, near the source end of the channel the current

degradation due to the presence of a negatively charged double trap is large because the double trap introduces additional barrier for the current flow. When the double trap is in the middle section of the channel, the current degradation is smaller. Traps near the drain contact, where the electron density is pinched off for the bias conditions used, are not effectively screened and a notable increase of the current degradation is observed. At the drain contact, the degradation drops practically to zero because there traps are effectively screened by the electrons. The expected current trends under small and large drain voltages are explained in Fig. 14.

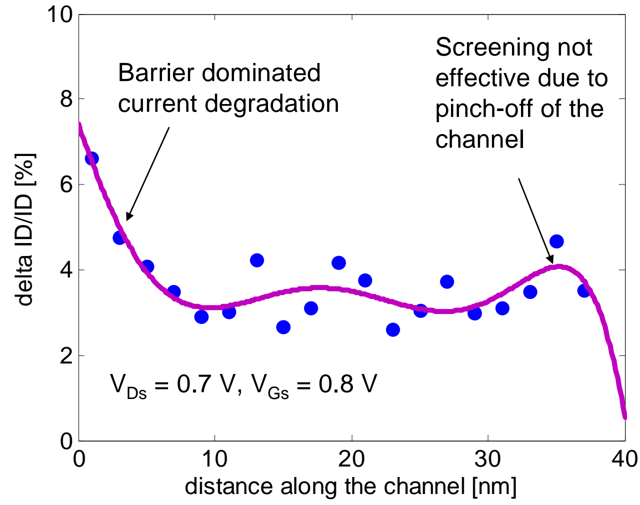

Figure 13. ON-current degradation vs. trap position. The statistical ensemble used here consists of the first 7 devices from Figure 9 with different number and different distribution of the impurity atoms.

4. Conclusions

Unlike most of the analytical revelation of published articles, where it has been reported that fluctuation in drain current amplitude variation and threshold voltage variation tend to diminish at strong inversion and saturation conditions imposing higher gate and drain bias owing to the screened out potential due to high inversion charge density at the surface with associated improvement of Coulombic-scattering related mobility, our simulations conducted at saturation bias conditions on a 45 nm MOSFET reveal that for different random dopant distributions in the channel and bulk, the fluctuation pattern exhibited by drain current amplitude variation and threshold voltage variation are truly statistical and random in nature, i.e., for some specific random dopant distributions , the fluctuation na-

ture is well controlled whereas for some other random dopants, the fluctuation pattern shows significant transitions between local peaks and valleys. From our EMC simulation, it has been demonstrated that fluctuations in the drain current amplitude and the threshold voltage have been dependent on particular random dopant distribution type, i.e, its number within the channel area and its position, in addition to having strong correlation on strategically positioned interface traps along the channel from source to drain.

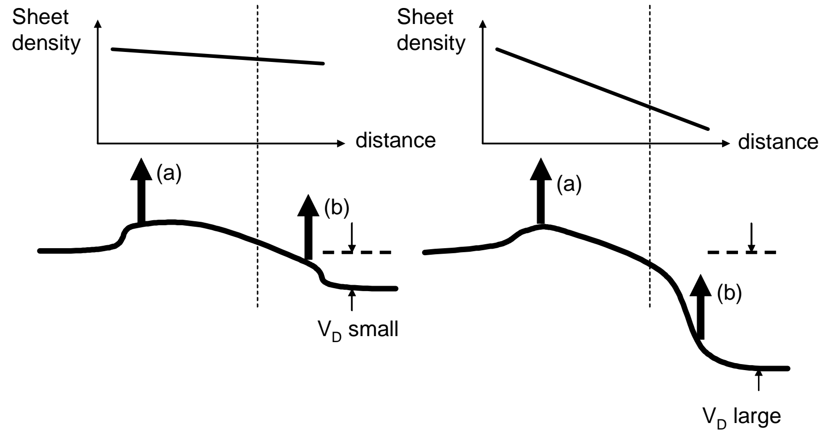

Figure 14. Under small gate and drain bias, we have the situation depicted in Fig. 12. For large gate bias: (a) the sheet density increases which means that screening increases; (b) traps near the drain are surrounded with large number of electrons for small V_D, therefore screening of the Coulomb potential is large and there is smaller degradation of the current; (c) for large V_D traps near the drain are surrounded with smaller number of electrons, therefore screening is smaller and we have slightly larger I_D degradation.

In order to truly represent the amplitude variation to show more dependence on spatial positioning of trap than specific random dopant type, the expectation value of the statistic (drain current or threshold voltage amplitude change) or the average term needs to be studied out of a significant number of possible random channel dopant distributions. These averaged-out values of drain current and threshold voltage fluctuations as extracted by the simulations can be analytically rationalized through the concept of device physics of scaled MOSFETs. We propose herein the following analytical physical explanations supporting the simulated results obtained for drain current fluctuations and threshold voltage fluctuations with associated fluctuations in its standard deviation induced by trap's occurrences in the channel close to the interface spatially located between source and drain.

4.1 Local Surface Potential Fluctuations

It has long been known that random dopant fluctuations cause fluctuations in the surface potential along the channel from source to drain and also from interface to some depth into the bulk. The fact that at strong inversion and saturation condition, the ready availability of inversion charge density smears out the surface potential variation, thus possible fluctuation in drain current and threshold voltage, needs a second look. With considerable scaling of gate length along with narrow width MOSFET devices, there are only few 100 atoms available per device area of scaled MOSFET and considering their random positioning along the channel and also along the depth from interface towards bulk, based on the fact that the depletion region available underneath the channel itself has a spatial random distribution owing to the random doping of the bulk, the inversion charge density formed by surface band bending is not continuous along the interface from source to drain, rather it is discrete and spatially random and nonuniform. Therefore the very possibility of screened out or smeared out surface potential at the interface is never a reality and depending upon the local fluctuation enhanced inhomogeneity of inversion charge density even at high gate bias, there will be sizeable spatial variation of surface potential at the interface from source towards drain. In addition to experiencing fluctuation due to random discreteness of channel dopant position and its number, the local surface potential fluctuation is also enhanced by the strategic location of trap or a number of traps interspersed between one another and distributed along the channel from source to drain. A repulsive trap center originating from the presence of acceptor like traps will enhance the spike in local potential amplitude at the trap's position and if this trap happens to be situated right at the source side or even a few nm away from the source side, the spike in potential barrier is going to significantly impede the carrier flow and thereby reduce the number of carriers that reach the drain side and contribute to current value. A trap's positioning at the source side being repulsive type consequently causes significant negative shift in current value and significant rise in fluctuation percentage value of relative drain current amplitude. This phenomenon is not uncommon in modern process controlled MOSFET fabrication as most RTF related phenomenon are caused by acceptor like traps being repulsive in nature. As the drain bias increases ensuring saturation conditions, the spatial conduction energy band gradually decreases towards the drain, enhancing drift related carrier transport where the carriers either enter the condition of velocity saturation or velocity overshoot near the drain zone and easily surmount any local barrier constituted surface potential fluctuation. Hence if the traps are near the drain side, the fluctuation pattern reduces to a steady and stable value. This physical aspect is corroborated by all the simulation outputs of present research work regarding drain current fluctuation. When the double-trap is located at the pinch-off region there is slight increase in the current degradation.

For the threshold voltage fluctuations and fluctuation in standard deviation of threshold voltage as extracted by our simulation results, the analytical explanation holds and since a trap's presence at the source side of the channel is causing maximum resistance to carrier flow by showing a peak of local surface potential at trap's position, therefore this will affect the inversion charge density available at

threshold and shift the threshold voltage by altering the gate bias conditions at threshold. Therefore relative threshold voltage amplitude reaches a high peak near source side trap positions and due to presence of high enough energetic carriers along the drain region, a trap's positioning there would not alter the inversion condition to the extent that a considerable shift in threshold voltage amplitude will be expected. Hence, the threshold voltage shift for drain side-positioned traps will be minimal. This physical aspect is also vindicated by the available data statistics that have been shown in the plots shown previously for threshold voltage variation with its fluctuation in standard deviation of threshold voltage. The explanation presented in this subsection from device physics standpoint is attributed to the condition that a large number of channel random dopant distributions are considered and have been averaged to arrive at the values of final drain current fluctuation statistic and threshold voltage fluctuation statistic. Expectedly, the randomness of the distribution of channel and bulk dopants will induce comprehensive randomness in local surface potential fluctuations making the after effect on the drain current fluctuations and threshold voltage fluctuations to be purely statistical. In essence, the plots shown with different random dopant distributions related drain current amplitude fluctuation and threshold voltage variation reveal a very important observation that strategically devised random channel dopant distributions through ion implantation can more successfully suppress the variability in drain current and threshold voltage and excel against RTF related device failure.

4.2 Fluctuation in Carrier Mobility

Each trap acts as a potential scattering center and impacts the scattering related transport efficiency. When the traps are closely apart and randomly positioned along the channel from source to drain, trap's interaction with carrier electron in the inversion channel and fixed ions in the underlying depletion region modifies the short range trap-to-electron-electron and trap-to-electron-ion Coulombic potential giving rise to significant Coulomb scattering related mobility reduction. Since our EMC transport kernel is equipped with properly accounting for this Coulomb effect, the results of the simulations perfectly reveal the fact that due to the random reduction of transport mobility of carrier due to trap's position and interactions with nearby electrons and ions, drain current amplitude reduction and hence larger fluctuation of drain current amplitude is expected which will be spatially nonuniform. The Coulomb related short range and long range e-e and e-ion interaction with traps will also result in significant threshold voltage shift at inversion condition on the gate, hence is responsible for trap related threshold voltage fluctuation. The modification of Coulomb potential seen by a trap surrounding its vicinity where a significant or no carrier may reside and significant or no ion may reside stemming from their mutual random and discrete nature, is also severely impacted by a trap's proximity to a nearby trap. Since for all our simulations, the traps were very closely positioned to one another within 1 nm separation, this will induce more Coulomb potential change and changes in local short range trap-electron and trap-ion interaction affecting carrier mobility. The rapid screening of Coulomb potential only occurs at the drain side with high bias on drain and hence

at those locations (except the pinch-off region), mobility reduction is minimal and the fluctuation pattern for both relative drain current and threshold voltage is minimized. In addition, depending on the discrete positioning and number density of channel dopants, the particular trap-to-electron and trap-to-ion interaction for both short and long range Coulomb forces will be fully distinctive and random causing randomness in mobility reduction spreading over different random channel and bulk dopant distributions. Larger spikes and surges in local surface potential values expected near the source side, will contribute to associated variation in short range and long range Coulomb force related scattering probability of carrier transport for a trap positioned there.

4.3 Interface Conditions

From the EMC simulation results of our present research work on RTF related drain current and threshold voltage fluctuation, a close observation reveals the important viewpoint that for interface trap occurrences, only traps within a thousandth fraction of a nm from the interface in the channel are considered for study. It has been shown by the exhaustive work of Professor Dragica Vasileska and her co-researchers that both the drain current and threshold voltage are strongly correlated to within a few nm from the interface to the vertical channel depth. Since the traps designed in our simulation are almost within a considerable fraction of a nm from the interface, it is vindicated from previous simulation study with present EMC code that both drain current fluctuation pattern and threshold voltage fluctuation pattern will show strong positive correlation with trap's proximity to the interface. This feature has been found to be another potent factor for reasoning out wide fluctuation patterns observed for both drain current amplitude and threshold voltage variation with its standard deviation. In addition, the interface roughness and chemical imperfections due to trap's positioning as scattering centers at random locations from source to drain are also a significant source for interface roughness scattering related mobility reduction which from theory is found to be one of most dominant causes for mobility reduction at high gate and drain bias, i.e. saturation bias condition of the MOSFET which we employed in our simulation for on current fluctuations study. The interface roughness will reduce the overall effective mobility with the traps acting as scattering sites randomly distributed within the inversion channel, being in conjunction with Coulomb-force related mobility reduction and will impact spatial random and statistical variation in both relative drain current amplitude.

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