Resonant Tunneling Diode Simulation

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1. In this problem, we will use software on *nanoHUB.org* to plot the I-V characteristic of a resonant tunneling diode. Visit the following page:

   https://www.nanohub.org/simulation_tools/rtd_tool_information

   Please use the following parameters:

   a) 2-barrier device
   b) Barrier thickness ($Al_{0.3}GaAs$): 5nm
   c) Well thickness (GaAs): 5 nm
   d) Temperature: 300 K
   e) Doping at contacts: $10^{18}/cm^3$

   Plot the I-V characteristic for V=0 ~ 0.4 volt. What are the values of I_p & I_v?

   p.s. DON'T turn the self-consistent potential on

2. In the previous homework, we have learned how to use the RTD software on *nanoHUB.org*. Design a RTD that gives the largest PVCR (peak-to-valley current ratio). You can adjust any parameter in the simulator, and again, DON'T turn on the self-consistent analysis.

   Explain why and how you choose your parameters to maximize the PVCR.

3. Consider the RTD-based SRAM circuit discussed in class (see *IEEE Transactions on Nanotechnology, Vol. 4, No. 4, p.472 (2005)*). We are going to do some simplified analysis to "design" a RTD SRAM.

   For a typical DRAM the storage capacitance is 35 fF (C_o = 35 fF). Assume the bit line capacitance is 0.2 pF/mm and the bit line is 300 μm long. Also assume the leakage current of the storage node is 0.5 pA per cell.

   By using the RTD simulator on *nanoHUB.org*, design a RTD that will result into a working SRAM cell (you may use the results from the homework as a starting point). You have to answer the following questions:

   a) What is the layer structure, i.e. material and thickness of your RTD?
   b) What is the area of the RTD required?
   c) If the area of a typical DRAM cell is $6F^2$ where F = half-pitch of the technology (typically identified as the "technology node"), will the area of your RTD fits on top of the DRAM cell for F = 130 nm, 90 nm, 65 nm, 32 nm, 22 nm technology? Ignore the problem of wiring the RTD for this exercise.
   d) What are the voltages of the two stable points (V_L, V_H) of the storage cell? Show how you determine the V_L, V_H and whether the cell is stable upon reading the cell (read "0" and "1").
   e) How can you make V_L and V_H closer to ground and V_{DD}?

f) What is the magnitude of the restoring current?

Notes:

To read the cell, the bit line is first charged to $V_{DD}/2$ ($V_{DD} = 2$ V) and then the word line is activated by turning on the access transistor. You need to make sure that the RTD does not get switched past the peak current, otherwise the NDR region will kick in and the memory state will be changed. Do not worry about the condition for writing the cell.

Assume the access transistor is F wide (where F = 130 nm, 90 nm, 65 nm, 32 nm, 22 nm) and the transistor delivers a current of 800 µA/µm (independent of technology node) when turned on with $V_{DD}/2$ across the source & drain terminals.

4. We would use the *MSL simulator* in this question. Login on the *nanoHUB.org* website and initiate the *MSL simulator*. Here is a quick demo of this simulator:

   https://www.nanohub.org/images/tool/msl/stanford-msl.swf

   Answer the following questions:

   a) What is the calculated bandgap of (4,2) nanotube? (Take 12 K-points and use Harrison parameterization)

   b) Use the formula on p.17 of CNT lecture notes to estimate the bandgap of (4,2) nanotube. Is there a difference compared with the answer in problem (a)?

5. For a zigzag CNT (Carbon NanoTube) i.e. (n,m)=(n,0):

   a) Derive the allowed k vectors.

   b) Derive the 1D dispersion relation.

   (HINT: see p.13 & p.14 of CNT lecture notes)