Network for Computational Nanotechnology (NCN)

University of California, Berkeley; University of Illinois at Urbana-Champaign; Norfolk State University; Purdue University; University of Texas at El Paso

First-Time User Guide to MOSCAP*

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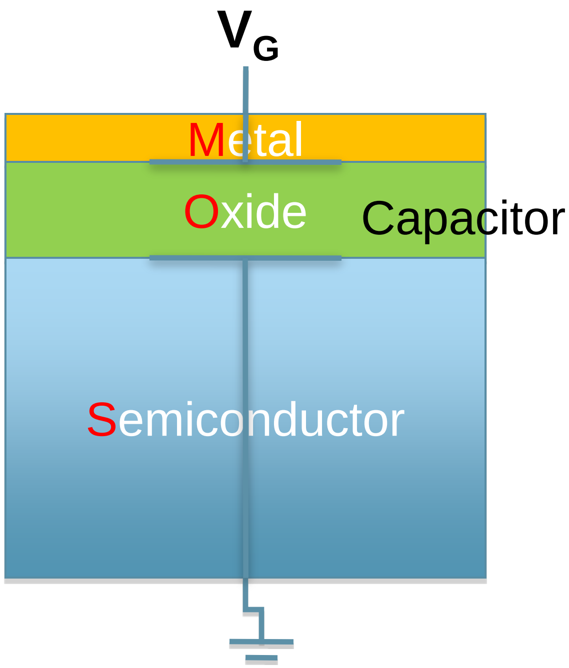
Table of Contents

- Introduction 3
  - →What is a MOS Capacitor ?
  - →What can be measured in MOS Capacitors?
- What Can Be Simulated by MOSCAP?: input 5
- What If You Just Hit the “Simulate” Button?: output 8
- Examples of Simulation Runs (input-output relationship) 10
  - →What if the doping in the semiconductor is changed?
  - →What if the oxide thickness is changed?
- What is PADRE?: the simulator behind MOSCAP 13
- Limitations of the MOSCAP Tool 14
- References 15

Introduction: What is a MOS Capacitor?

MOS Capacitor: Metal Oxide Semiconductor[1] Capacitor



- Metal : metal or poly-silicon material
- Oxide : SiO_2 or high-κ dielectric material
- Semiconductor : p-type or n-type semiconductor material

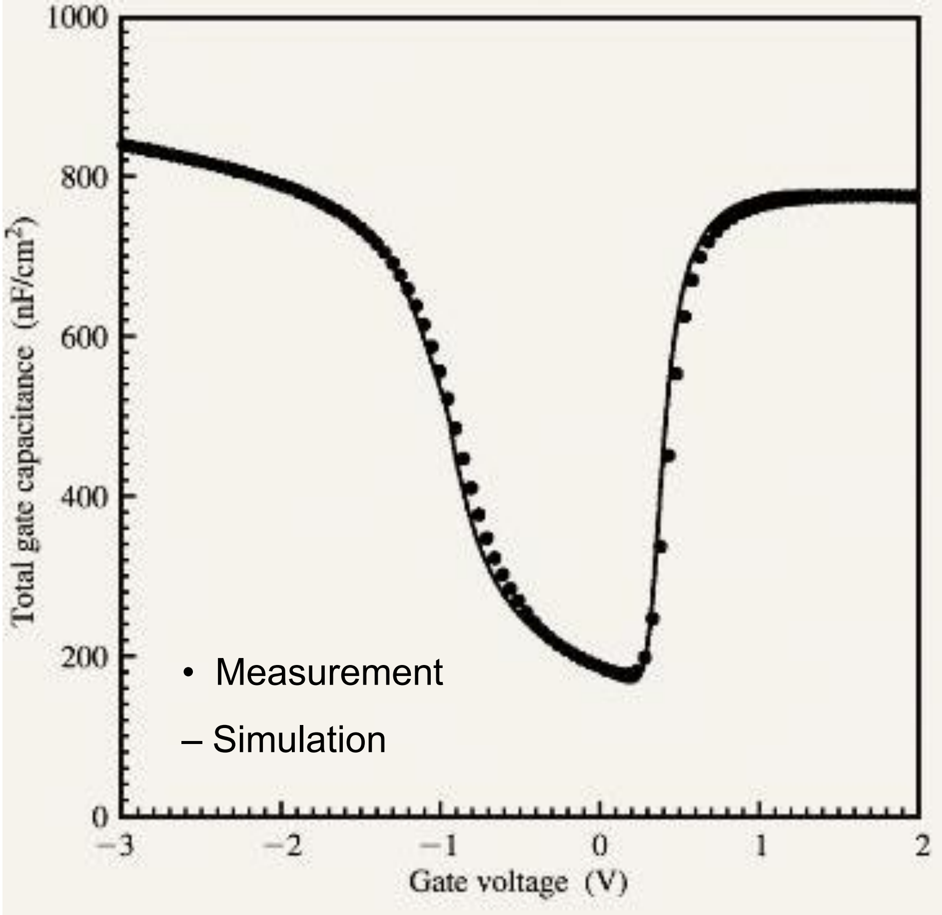
- Importance of MOS Capacitors
  - » Essential for understanding MOSFET*[2]
  - » Basic structural part of MOSFET

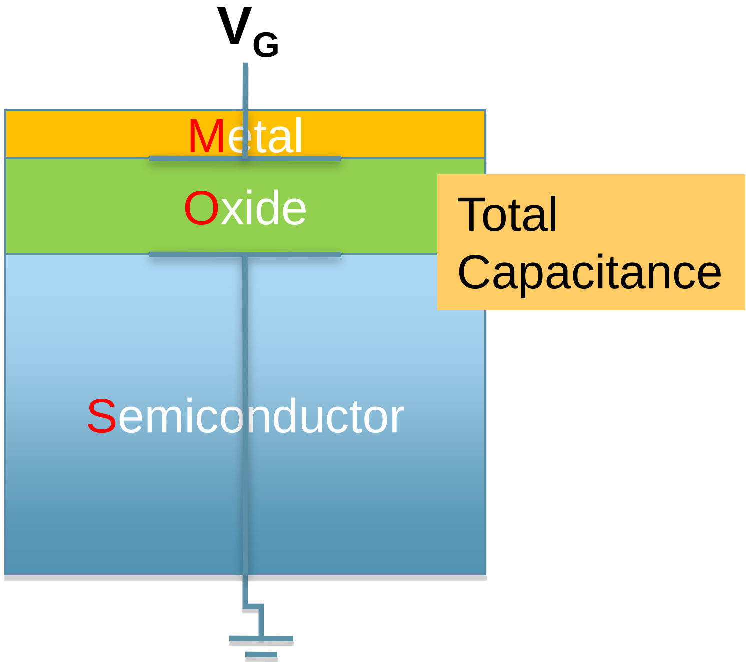
[1] Dragica Vasileska (2008), "MOS Capacitors Description," http://nanohub.org/resources/5087

*MOSFET : Metal Oxide Semiconductor Field Effect Transistor has a source and a drain as an additional contacts to the gate contact as shown in the picture above.
For more information, refer to the following reference [2]
[2] Dragica Vasileska (2008), "MOSFET Operation Description," https://nanohub.org/resources/5085

Introduction: What Can Be Measured in MOS Capacitors?

Capacitance-Voltage Characteristics[3]



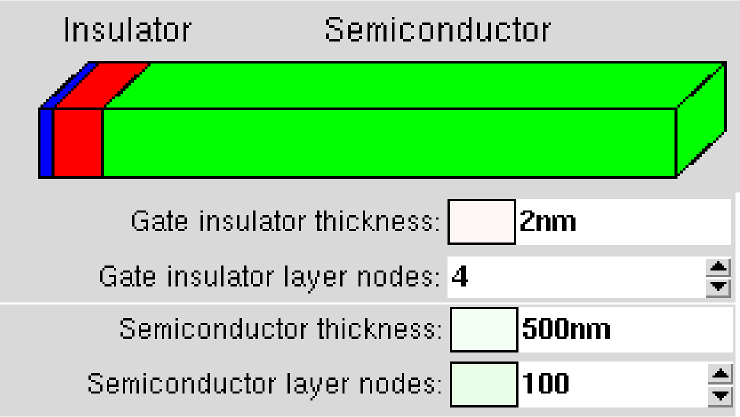


[4] S.-H. Lo, et. al., IBM Journal of Research and Development, volume 43, number 3, 1999

What Can Be Simulated by MOSCAP? (input):

MOS Capacitor with different geometry

Single Gate



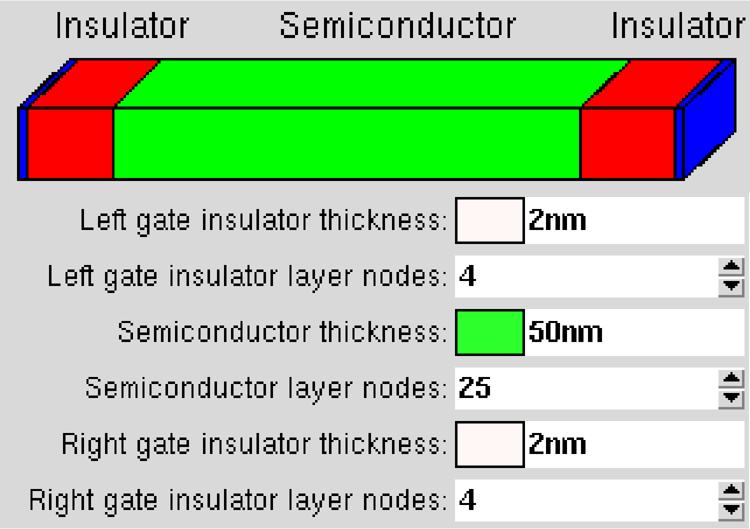
Gate insulator thickness: 2nm

Gate insulator layer nodes: 4

Semiconductor thickness: 500nm

Semiconductor layer nodes: 100

Double Gate



Left gate insulator thickness: 2nm

Left gate insulator layer nodes: 4

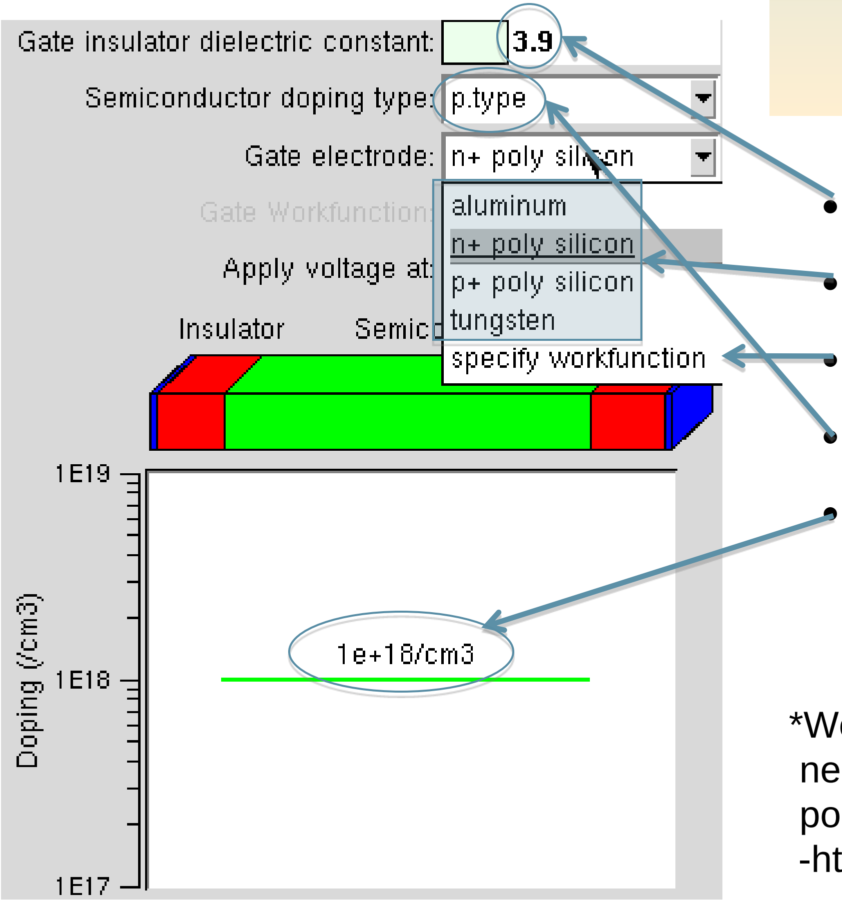
Semiconductor thickness: 50nm

Semiconductor layer nodes: 25

Right gate insulator thickness: 2nm

Right gate insulator layer nodes: 4

What Can Be Simulated by MOSCAP? (input):


Gate insulator dielectric constant: 3.9

Semiconductor doping type: p.type

Gate electrode: n+ poly silicon

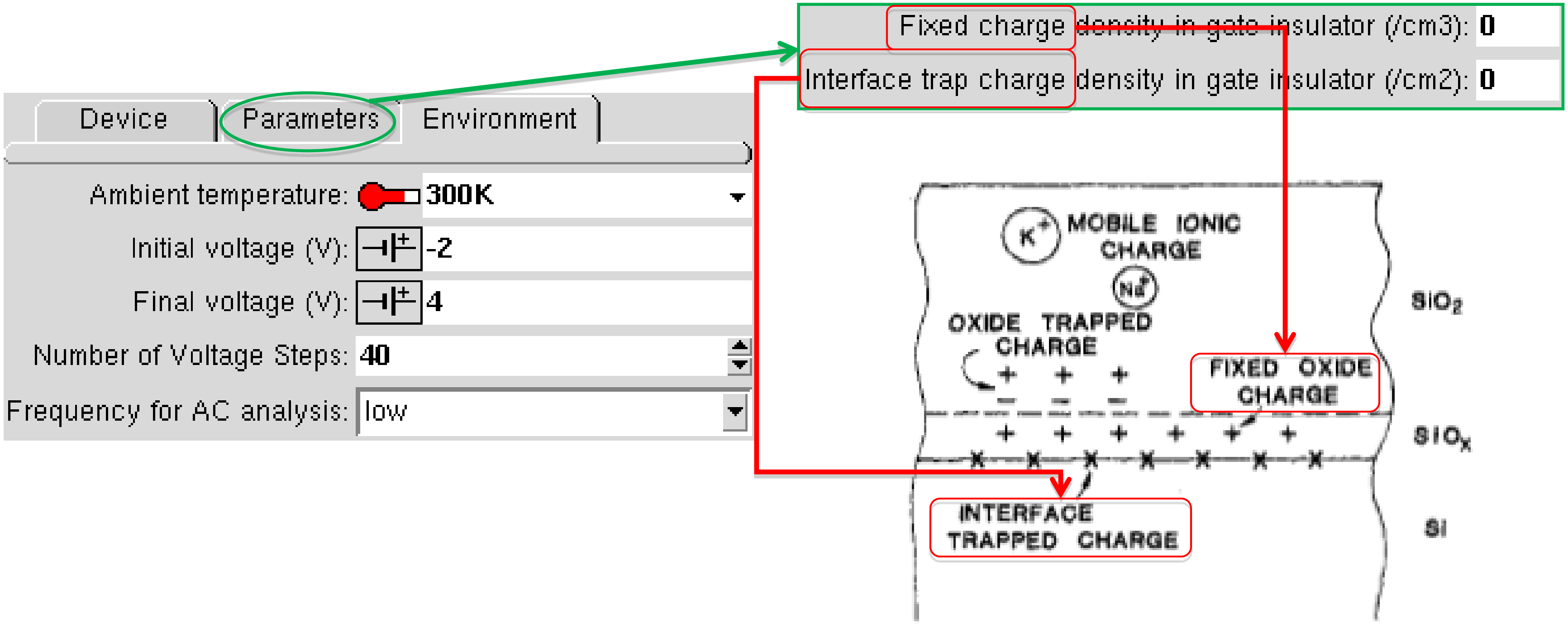
MOS Capacitor with different doping and material

- Insulator dielectric constant
- Gate electrode type
- Gate workfunction* specification
- Semiconductor doping type
- Semiconductor doping density

*Workfunction is the minimum energy that is needed to remove an electron from a solid to a point immediately outside the solid surface -http://en.wikipedia.org/wiki/Work_function

What Can Be Simulated by MOSCAP? (input):

- Environment parameters
- Special parameters(charge density in the insulator)



Fixed charge density in gate insulator (/cm3): 0

Interface trap charge density in gate insulator (/cm2): 0

Ambient temperature: 300K

Initial voltage (V): -2

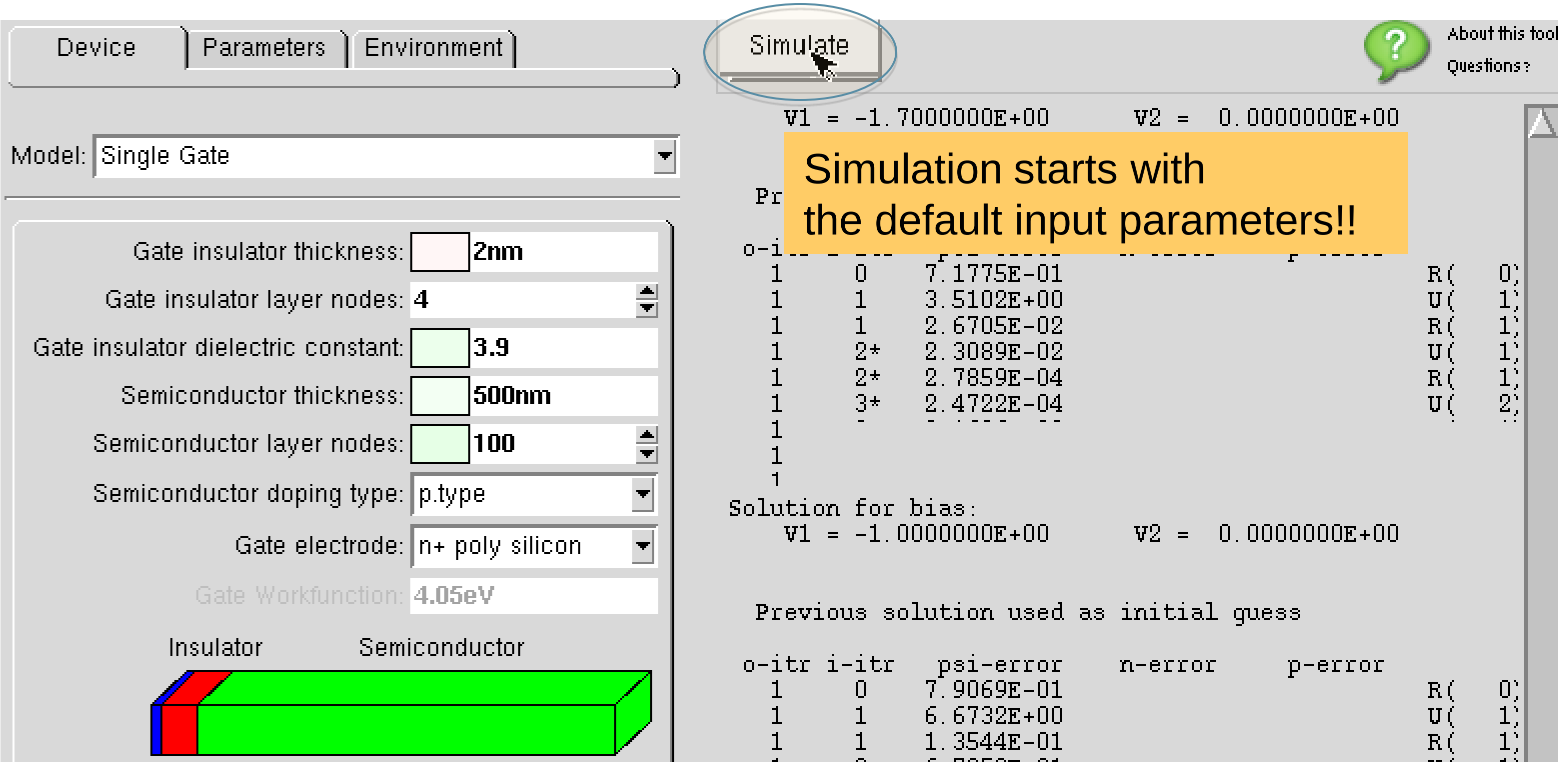
Final voltage (V): 4

Number of Voltage Steps: 40

Frequency for AC analysis: low

[5]Deal B. E., Electron Devices, IEEE Transactions on, 1980

What If You Just Hit the “Simulate” Button? (output):



Model: Single Gate

Gate insulator thickness: 2nm
Gate insulator layer nodes: 4
Gate insulator dielectric constant: 3.9
Semiconductor thickness: 500nm
Semiconductor layer nodes: 100
Semiconductor doping type: p.type
Gate electrode: n+ poly silicon
Gate Workfunction: 4.05eV

```
    V1 = -1.7000000E+00       V2 =  0.0000000E+00


  Pr

 o-i
  1     0    7.1775E-01                                  R(   0)
  1     1    3.5102E+00                                  U(   1)
  1     1    2.6705E-02                                  R(   1)
  1     2*   2.3089E-02                                  U(   1)
  1     2*   2.7859E-04                                  R(   1)
  1     3*   2.4722E-04                                  U(   2)
  1
  1
  1
Solution for bias:
    V1 = -1.0000000E+00       V2 =  0.0000000E+00


  Previous solution used as initial guess

 o-itr i-itr   psi-error    n-error     p-error
  1     0    7.9069E-01                                  R(   0)
  1     1    6.6732E+00                                  U(   1)
  1     1    1.3544E-01                                  R(   1)
```

Simulation starts with
the default input parameters!!

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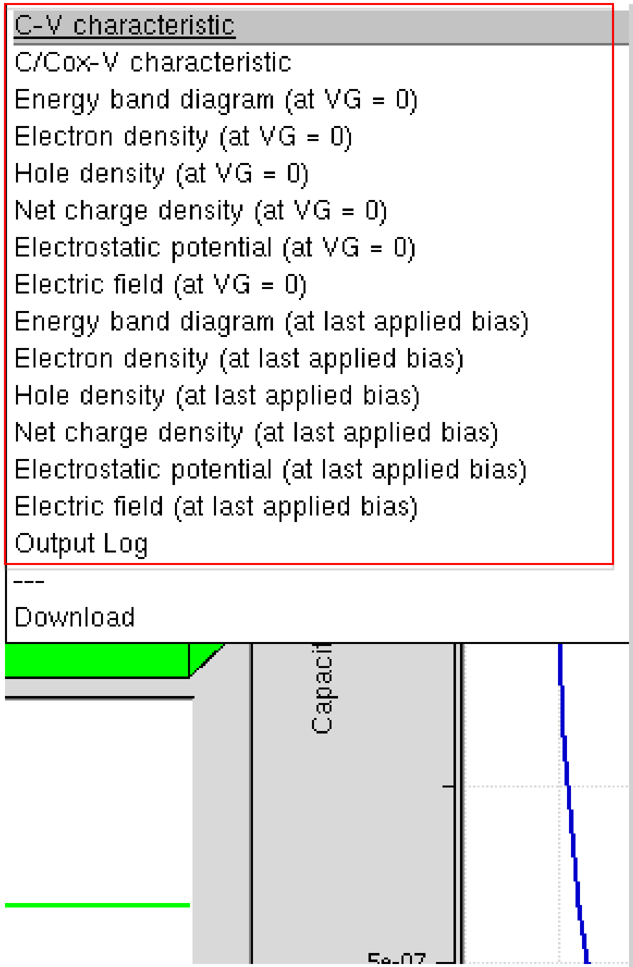
What If You Just Hit the “Simulate” Button? (output):

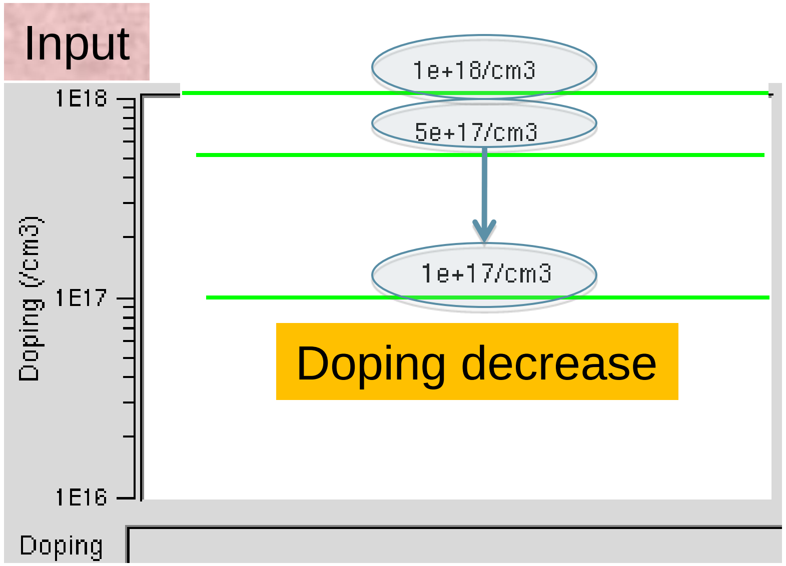


- [**C-V Characteristics**] : Gate capacitance vs Voltage characteristics
- [**C/Cox-V Characteristics**] : Gate capacitance devided by oxide capacitance vs Voltage characteristics
- [**Energy band diagram**] : Conduction/Valence Band, Fermi level diagram
- [**Electron density**] : electron density in the semiconductor
- [**Hole density**] : hole density in the semiconductor
- [**Net charge density**] : $\rho=q(N_A-N_D+n-p)$
- [**Electrostatic potential**] : $V = const-q\cdot E_c$
- [**Electric field**] : $E = -\nabla V$

ρ : *charge density*
N_A/N_D: *acceptor/Donor density*
n/p : *electron/hole density*
q : *electron charge*
Ec *conduction band edge*
E : *electric field*
V : *electrostatic potential*

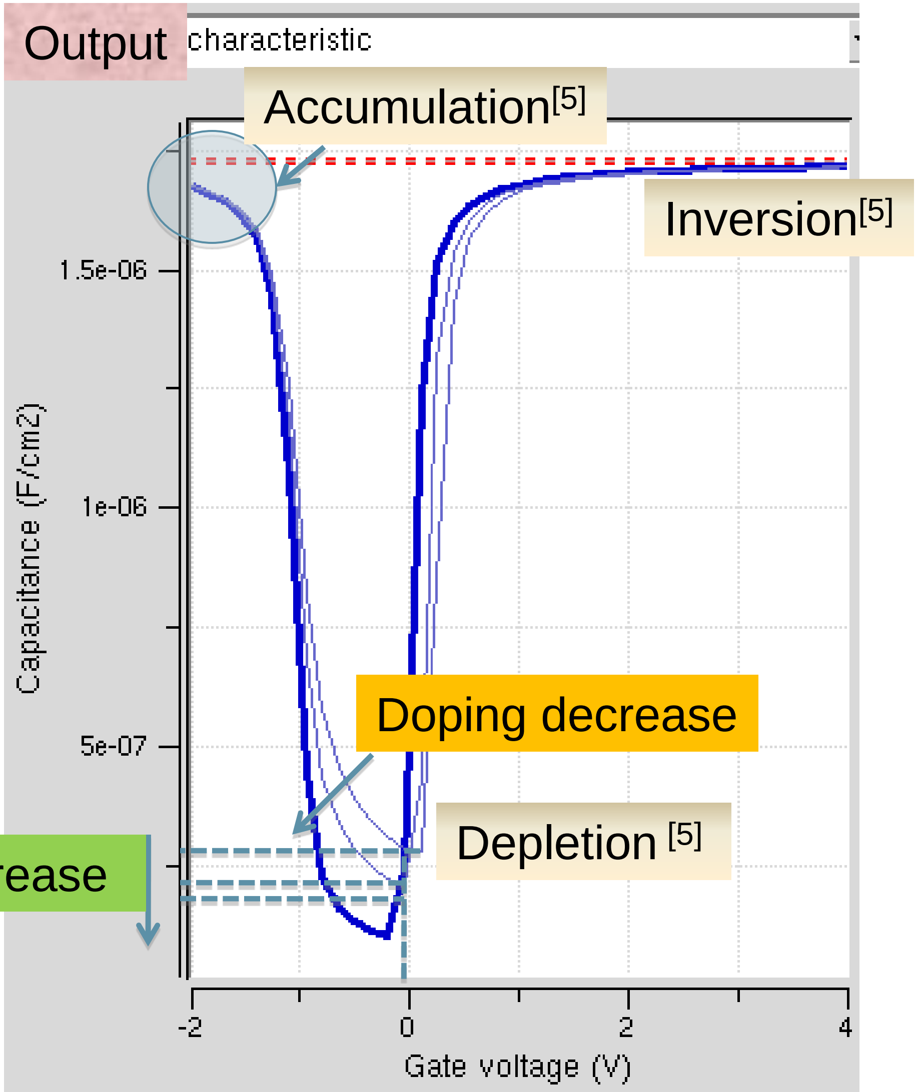
Example of Simulation (if the doping is changed)

Input



Doping decrease

Output



Accumulation[5]

Inversion[5]

Doping decrease

Depletion [5]

$C_{tot}|_{VG=0}$ decrease

[5] Mark Lundstrom (2008), "ECE 612 Lecture 3: MOS Capacitors," http://nanohub.org/resources/5363

Example of Simulation (if the doping is changed)

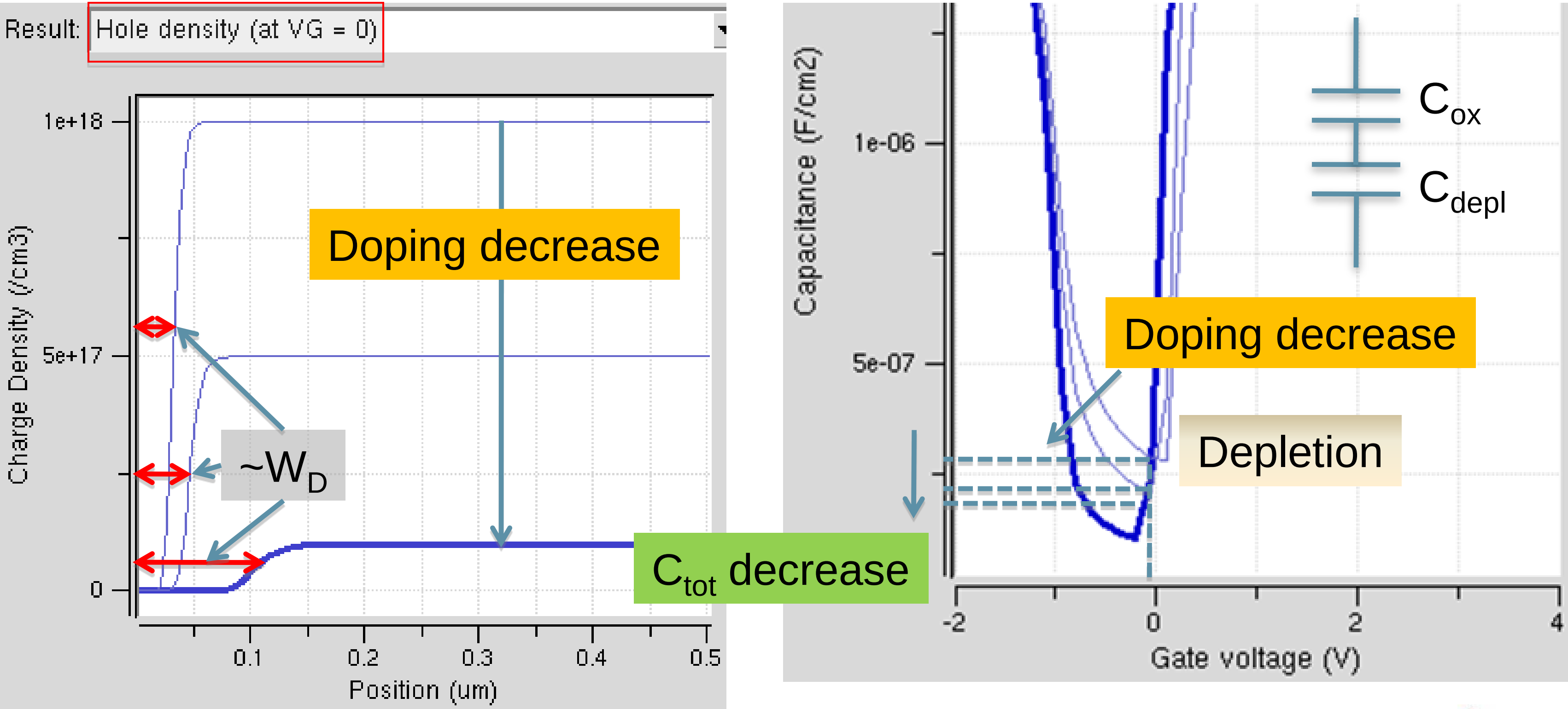
$$C_{tot} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{Depl}}}, \quad C_{depl} = \frac{\varepsilon_S}{W_D}, \quad C_{ox} = \frac{\varepsilon_{ox}}{d_{ox}}$$

$C_{tot} / C_{ox} / C_{depl}$: total/oxide/depletion capacitance

$\varepsilon_{ox} / \varepsilon_S$: dielectric constant of oxide/semi conductor

W_D : depletion width, d_{ox} : oxide thickness

W_D increase → C_{depl} decrease → C_{tot} decrease



Result: Hole density (at VG = 0)

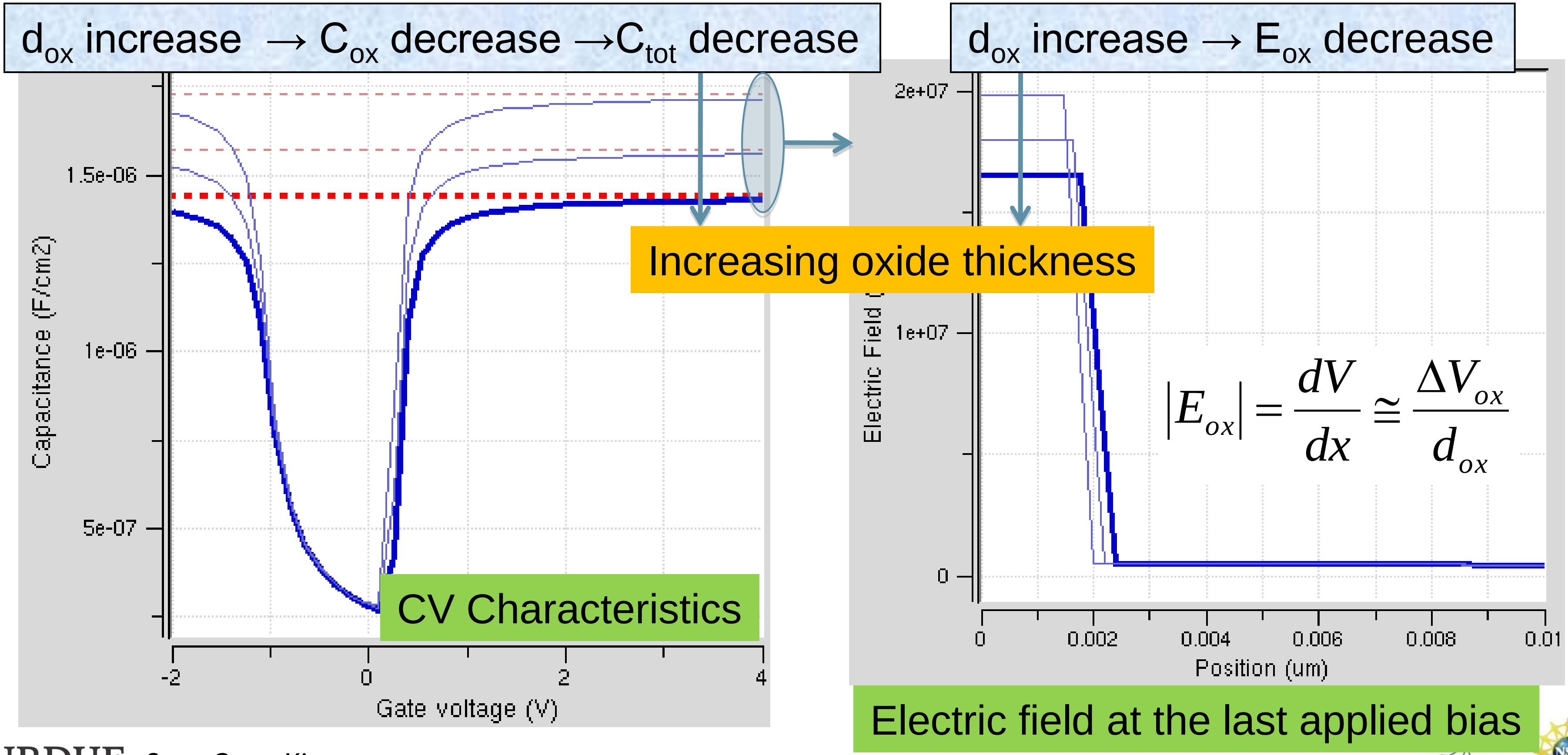
Example of Simulation (if the oxide thickness is changed)

$$C_{tot} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_S}}, C_{ox} = \frac{\varepsilon_{ox}}{d_{ox}}$$

$C_{tot} / C_{ox} / C_S$: total/oxide/semiconductor capacitance

$\varepsilon_{ox} / \varepsilon_S$: dielectric constant of oxide/semi conductor

W_D : depletion width, d_{ox} : oxide thickness



d_{ox} increase → C_{ox} decrease → C_{tot} decrease

d_{ox} increase → E_{ox} decrease

Increasing oxide thickness

$$|E_{ox}| = \frac{dV}{dx} \cong \frac{\Delta V_{ox}}{d_{ox}}$$

CV Characteristics

Electric field at the last applied bias

What is PADRE?: the simulator behind MOSCAP

PADRE[6] : classical drift-diffusion simulator

- PADRE simulates the electrical behavior of devices under steady state, transient conditions or AC small-signal analysis[7].

Self consistent simulation

Poisson equation

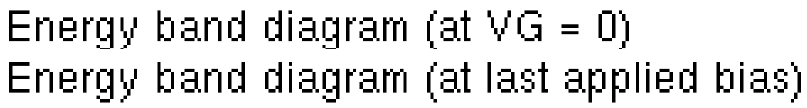
Drift-diffusion equation

[6] Dragica Vasileska; Gerhard Klimeck (2006), "Padre," DOI: 10254/nanohub-r941.3.

[7] http://nanohub.org/resource_files/tools/padre/doc/index.html

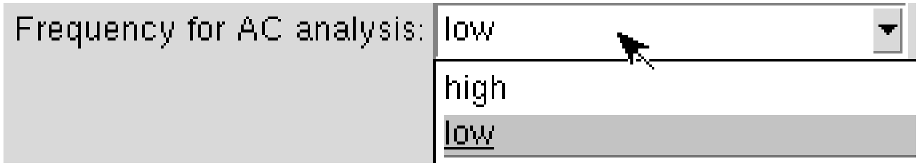
Limitations of the MOSCAP Tool

- MOSCAP does not model quantum mechanical effects
  - Confinement of carriers in the semiconductor
  - Tunneling from the gate to the semiconductor
- MOSCAP does not have sequence plots – users cannot see what happens in the intermediate steps between V_G=0 and the last applied bias*



Energy band diagram (at VG = 0)
Energy band diagram (at last applied bias)

- MOSCAP does not allow users to choose the frequency for AC analysis*



Frequency for AC analysis: low

* These features may be upgraded in the next versions.

References

- MOS Capacitor/MOSFET basic theory

[1] www.eas.asu.edu/~vasilesk, Dragica Vasileska (2008), "MOS Capacitors Description," http://nanohub.org/resources/5087

[2] www.eas.asu.edu/~vasilesk, Dragica Vasileska (2008), "MOSFET Operation Description," https://nanohub.org/resources/5085

[3] Mark Lundstrom (2008), "ECE 612 Lecture 3: MOS Capacitors," http://nanohub.org/resources/5363

- MOS Capacitor C-V measurements

[4] S.-H. Lo, et. al., IBM Journal of Research and Development, volume 43, number 3, 1999

- Charges in oxide

[5] Deal B. E., Electron Devices, IEEE Transactions on, 1980

- PADRE

[6] Dragica Vasileska; Gerhard Klimeck (2006), "Padre," DOI: 10254/nanohub-r941.3.

[7] http://nanohub.org/resource_files/tools/padre/doc/index.html