Chapter 1

MOSCap Tool on nanoHUB.org: A Primer

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The primary reason to study MOS (metal-oxide-semiconductor) capacitors is to understand the principle of operation as well as become familiar with some of the routinely used characterization techniques for MOS field effect transistors (MOSFETs). The MOSCap tool on nanoHUB.org simulates the one-dimensional electrostatics in single and dual-gate MOS device structures along the growth direction as a function of device dimension, oxide charge, temperature, doping concentration, and AC frequency. Among the quantities simulated, the low and high-frequency capacitance-voltage (CV) characteristics and various spatial profiles (energy band, electric field intensity, charge densities, and surface potential) are of special importance. In this chapter, we will describe: 1) Structure and basic operational principle of an MOS capacitor; 2) User interface of the MOSCap simulator; 3) How to prepare an input deck and sample simulations (examples); 4) Outputs and the major technologically important information that can be extracted from the simulation results; and 5) Limitations of the MOSCap tool. The chapter is expected to increase comprehension of the operation and applications of both conventional and novel MOS capacitors from a semi-classical viewpoint. For a quantum-mechanical description of capacitance in a MOS structure, please see the Chapter on the *Schred* tool.

1. Introduction

1.1. *What is an MOS Capacitor?*

A capacitor is a device used to store electric charge. In its simplest form, it consists of a pair of conductors separated by an insulator (dielectric material). The MOS capacitor consists of a metal-oxide-semiconductor

structure as shown in Fig. 1 below. The top layer is a metal or heavily doped (on the order of $10^{20} cm^{-3}$) poly-silicon layer (which acts as a metal). A thin oxide (here, SiO_2) layer is sandwiched between the top conducting layer and a bulk semiconductor (here, silicon) substrate that sits below the insulator. The substrate, which is tied to the ground in normal mode of operation, could be doped either p-type or n-type.

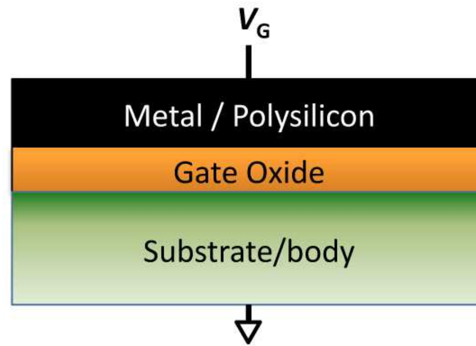


Fig. 1. A simple MOS capacitor.

1.2. *Terminologies*

Before we describe the operating principle of the device, we need to familiarize ourselves with some terminologies. Below is a list:
Vacuum Level: It is the energy level where the electrons are free.
Electron Affinity (χ): Energy required for an electron to break loose from atom and go to the vacuum level.
Fermi Level (E_f): It is the energy level where the probability of finding an electron is $\frac{1}{2}$. Fermi level provides useful information on how the electrons are distributed in the energy space.
Work Function ($q\Phi$): The energy difference between the vacuum level and the Fermi level of any material. It is generally unique for a given material.
Band Gap (E_g): The energy difference between the conduction band, E_c, and the valence band, E_v, of a semiconductor.
Intrinsic Level (E_i): The energy level that lies at the center of the band gap such that $E_i = (E_c - E_v)/2$.

2. The Ideal MOS Capacitor

Let us consider an ideal p-substrate MOS capacitor (for a useful review see Ref [1]). To accurately characterize MOS devices, we need to understand the energy band diagrams. The energy band diagram of an ideal MOScap in equilibrium (unbiased) condition is shown in Fig. 2. For an ideal MOSCap, the metal workfunction ($q\Phi_m$) and the semiconducting workfunction ($q\Phi_s$) are equal. Hence, the Fermi levels (E_{fm}, E_{fs}) line up throughout the structure and all the energy levels remain flat (that is, no built-in fields within the structure). The quantity $q\phi_f$ in Fig. 2 measures the position of the Fermi level with respect to the intrinsic level of the semiconductor and, therefore, is a strong function of the substrate doping concentration. At room temperature ($T = 300$ °K) the bandgap of the SiO_2 is ~ 8.9 eV and that of silicon is ~ 1.12 eV. The substrate is grounded.

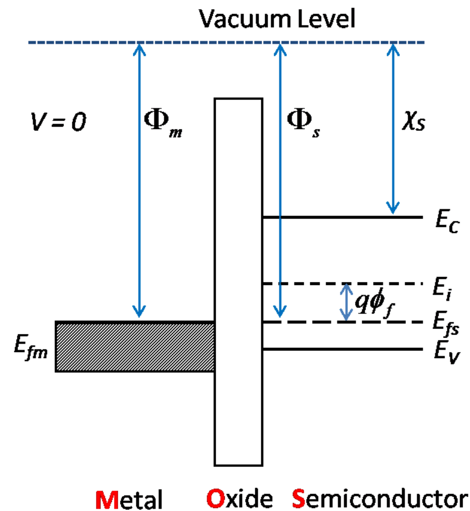


Fig. 2. Energy band diagram of an ideal MOS capacitor in equilibrium.

2.1. *Operation*

The simple band diagram as depicted above is modified when a voltage, V_g, is applied on the gate contact. Part of V_g is dropped across the oxide, V_{ox}, and part across the semiconductor, known as the surface potential, ϕ_s.

Depending on the polarity and magnitude of the applied gate voltage, the surface condition changes, and the MOSCap goes through *three* distinct operating regions as shown in Fig. 3. A negative gate voltage increases the positive charge density (holes in this case) on the substrate (accumulation mode); whereas a positive gate voltage creates a space-charge region at the oxide/semiconductor interface (depletion mode) and the thermally generated electrons start to populate the conduction band. As the positive gate voltage is further increased, the intrinsic level at first crosses the Fermi level (weak inversion) and eventually drops far below the Fermi level and the conduction band approaches the Fermi level. The density of electrons increases significantly and when the magnitude of the band bending (that is the surface potential) is equal to $2 \times q\phi_F$, we say that a complete (strong) inversion has occurred and a negatively charged electronic channel is formed. Note that, even when a nonzero gate voltage is applied (that is, the device is biased), since there is no current through the oxide insulator, the Fermi level remains flat across the structure. However, depending on the applied gate voltage and the surface condition, the direction of the electric field changes from negative to positive (as indicated in Fig. 3 with notation ξ). Also, note that Φ_m and χ are constants, and irrespective of the bias arrangements, the device always remains charge neutral.

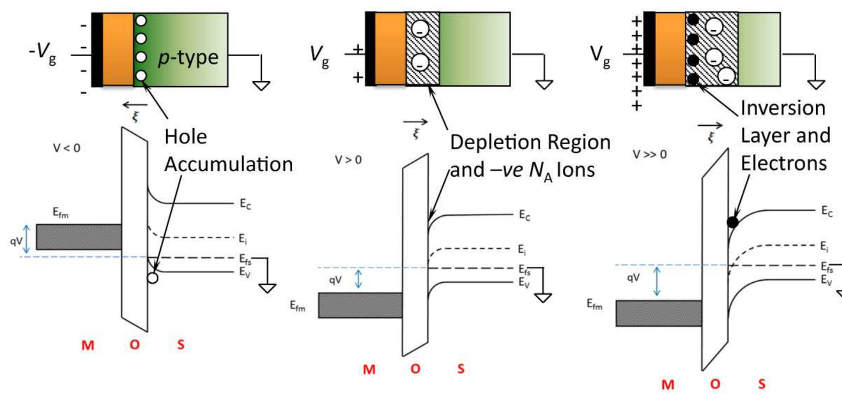


Fig. 3. Energy band diagram of an ideal MOS capacitor under applied bias. From left to right: accumulation, depletion, and inversion regimes.

2.2. *Analytical Calculation of Capacitance*

We know that capacitance is given by, $C = \frac{dQ}{dV}$, where Q is the charge and V is the potential. For an MOS capacitor, since $V_g = V_{ox} + \phi_s$, this equation can be written as:

$$C = \frac{dQ}{d(V_{ox} + \phi_s)} = \frac{1}{\frac{dV_{ox}}{dQ} + \frac{d\phi_s}{dQ}} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{sem}}} \tag{1}$$

Where, C_{ox} is the oxide capacitance and C_{sem} is the semiconductor capacitance originating from the response of the induced charge to the variation of the surface potential. In other words, we see that the total (net) capacitance of an ideal MOS capacitor comes from a series combination of C_{ox} and C_{sem}. To calculate the capacitance of an MOS device, therefore, we need to establish a relationship between the applied voltage and the induced charge in the semiconductor substrate. We can do this either analytically or through a numerical approach. The numerical approach involves the solution of the Poisson equation (most accurate in three dimensions), which is discussed in detail in the Chapter on PN Junction Lab. Here, we present the relevant equations for the semiconductor charge and the surface potential.

Charge in semiconductor substrate is given by[1]

$$Q_s = \pm K_s \varepsilon_o \frac{kT}{qL_{Di}} F(U_s, U_F) \tag{2}$$

(+ve for positive gate voltage and -ve for negative gate voltage.)
Here,
K_s is semiconductor dielectric constant (11.7 for silicon),
ϵ_o is permittivity of free space,
k is the Boltzmann constant,
T is the temperature in Kelvin,
Intrinsic Debye length, $L_{Di} = \sqrt{\frac{kTK_s\varepsilon_o}{2q^2n_i}}$,
$U_F = \frac{\phi_F}{kT}$,
$U_s = \frac{\phi_s}{kT}$,
$\phi_F = kTln\left(\frac{N_A}{n_i}\right)$,
n_i is the intrinsic doping density and
$F(U, U_F) = \sqrt{e^{U_F}(U + e^{-U} - 1) - e^{-U_F}(U - e^U - 1)}$.
Eq. 2 gives us the total charge as a function of applied potential.

The gate voltage is given by:
$V_g = \pm \frac{K_s T_{ox} kT}{K_{ox} q L_{Di}} F(U_s, U_F) + \phi_s$
Where,
T_{ox} is the oxide thickness,
K_{ox} is the oxide dielectric constant, and
ϕ_s is the potential drop across semiconductor (surface potential).

Below we provide a MATLAB code that uses the above equations and plots (in Fig. 4) the $Q_s - V_g, \phi_s - V_g$ and the $C - V_g$ characteristics (which seems to be noisy because of the discretization error) for an n-MOSCap structure.

```
%%% MOS capacitor electrostatics: p-substrate

%%% Clear workspace:
clc
clear

%%% Inputs:
Tox = 2e-9;
Na = 1e23;
q = 1.6e-19;
Ks = 11.7;
Kox = 3.95;
k = 1.38e-23;  %% J/K
T = 300;
eps0 = 8.85e-12;
Nc = 2e25;
Nv = 1e25;
Eg = 1.1;      %% in eV
Eg = 1.1*q     %% in Joules (J)

%%% Calculation:
ni = sqrt(Nc*Nv)*exp(-Eg/(2*k*T))      %% Eg and kT are both
phiF = (k*T)*log(Na/ni)                %% in J in Joules
Ldi = sqrt((k*T*Ks*eps0)/(2*q*q*ni))   %% Joule based
                                       %% calculation
ii = 1;
%% -ve gate voltage
```

```
for Vg = -2:0.01:0            %% Vg is potential (Volts) here
xaxis(ii) = Vg;
for V = 1.2:-0.00001:-1.2
%% V is a numeric (iterative) variable
%% for calculating Vs in Volts
lhs = Vg;                    %% LHS of the K.V.L.
  u = V*q;                    %% u is in Joules
Fs = sqrt(exp(phiF/k/T)*(u/k/T + exp(-u/k/T) - 1)
- exp(-phiF/k/T)*(u/k/T - exp(u/k/T) + 1));
rhs = -(Ks*Tox)/Kox * (k*T)/q * 1/Ldi * Fs + V;
%% RHS of the K.V.L. (-ve for -ve Gate voltage)
if(lhs/rhs>= 0.99 && lhs/rhs<= 1.01)
  Vs = V;
  %% Vs (surface potential) is in Volts
Fss = Fs;
end
end
Qs(ii) =  (Ks*eps0)*(k*T)/q*1/Ldi*Fss/q;   %% #/cm2;
yaxis(ii) = Vs;
%%yaxis is surface potential (volts)
ii = ii + 1;
end

%% +ve gate voltage
for Vg = 0:0.01:2             %% Vg is potential (Volts) here
xaxis(ii) = Vg;
for V = -1.2:0.00001:1.2
%% V is a numeric (iterative) variable for
%% calculating Vs in Volts
lhs = Vg;                     %% LHS of the K.V.L.
  u = V*q;                    %% u is in Joules
Fs = sqrt(exp(phiF/k/T)*(u/k/T + exp(-u/k/T) - 1)
- exp(-phiF/k/T)*(u/k/T - exp(u/k/T) + 1));
rhs = (Ks*Tox)/Kox * (k*T)/q * 1/Ldi * Fs + V;
%% RHS of the K.V.L.(+ve for +ve Gate voltage)
if(lhs/rhs>= 0.99 && lhs/rhs<= 1.01)
  Vs = V;
  %% Vs (surface potential) is in Volts
Fss = Fs;
```

```
end
end
Qs(ii) =  -(Ks*eps0)*(k*T)/q*1/Ldi*Fss/q;   %% #/cm2
yaxis(ii) = Vs;
%% yaxis is surface potential (volts)
ii = ii + 1;
end

%%% Capacitance:
for n = 2:1:ii-2
Vgate(n) = xaxis(n);
cap(n) = -(Qs(n)-Qs(n-1))*q/(Vgate(n)-Vgate(n-1));
if(cap(n)<1e-10)
cap(n) = cap(n-1);
end
end

%%%% Figure Plotting
figure('Color','White');
h1=plot(xaxis,abs(Qs),'r');
%% Plotting the absolute charge as a
%% function of gate voltage
% Line options
set(h1,'linestyle','-');
set(h1,'linewidth',2)
% Figure options
set(gcf,'Colormap',pink);
% Axis options
axis tight;
set(gca,'color',[1 1 1]*1.0);
set(gca,'fontsize',12);
set(gca,'layer','top');
set(gca,'linewidth',2);
xlabel('Gate Voltage, V_G_S [V]','Fontsize',16);
ylabel('|Q_S|, [#/m^2]','Fontsize',16);
% save
saveas(h1,'pMOScap-Qs-Vgs.fig');
print pMOScap-Qs-Vgs.eps-deps;
```

```
%%%% Figure Plotting
figure('Color','White');
h1=plot(xaxis,yaxis,'r');
% Line options
set(h1,'linestyle','-');
set(h1,'linewidth',2)
% Figure options
set(gcf,'Colormap',pink);
% Axis options
axis tight;
set(gca,'color',[1 1 1]*1.0);
set(gca,'fontsize',12);
set(gca,'layer','top');
set(gca,'linewidth',2);
xlabel('Gate Voltage, V_G_S [V]','Fontsize',16);
ylabel('Surface potential, [V]','Fontsize',16);
% save
saveas(h1,'pMOScap-phiS-Vgs.fig');
print pMOScap-phiS-Vgs.eps-deps;

%%%% Figure Plotting
figure('Color','White');
h1=plot(Vgate,cap,'r');
%% Plotting the absolute charge
% Line options
set(h1,'linestyle','-');
set(h1,'linewidth',2)
% Figure options
set(gcf,'Colormap',pink);
% Axis options
axis tight;
set(gca,'color',[1 1 1]*1.0);
set(gca,'fontsize',12);
set(gca,'layer','top');
set(gca,'linewidth',2);
xlabel('Gate Voltage, V_G_S [V]','Fontsize',16);
ylabel('Capacitance, [F/m^2]','Fontsize',16);
% save
saveas(h1,'pMOScap-Cap-Vgs.fig');
```

```
print pMOScap-Cap-Vgs.eps-deps;
```

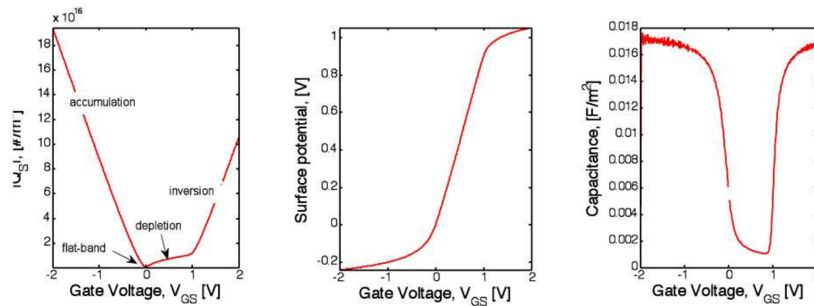


Fig. 4. $Q_s - V_g, \phi_s - V_g$, and the $C - V_g$ characteristics for an p-substrate MOS structure.

3. MOSCap Tool Description

The MOSCap simulator is available at (http://nanohub.org/resources/moscap). MOScap simulates the one-dimensional electrostatics in typical single and dual-gate MOS device structures along the growth direction as a function of device dimension, oxide charge, temperature, doping concentration, and applied frequency. Among the quantities simulated, the low and high-frequency capacitance-voltage (CV) characteristics and various spatial profiles (e.g., energy band, vertical electric field, charge densities etc.) are of special importance. MOSCap also has an option for plotting the semiconductor surface potential as a function of applied gate potential. In the following, we describe the input parameters, the output quantities, and important information that can be extracted from these outputs using the MOScap tool.

3.1. *Input Parameters*

To simulate a device, we need to consider several structural and other parameters in MOSCap. The input deck has four phases/tabs: *Device* (contains structural information), *Parameters*, *Environment* and *Surface Potential*.

3.1.1. *Device:*

Model: used to select Single or Double gate capacitor
Gate insulator thickness: Physical thickness of the oxide layer in μm (range: 0.001 - 10)
Gate insulator layer node: Number of finite calculation point in gate insulator layer (range: 0 - 350)
Gate insulator dielectric constant: Relative permittivity of dielectric material (ϵ_r)
Semiconductor thickness: Physical thickness of bulk semiconductor in μm
Semiconductor layer node: Number of finite calculation point (range: 2 - 1000)
Semiconductor doping type: Semiconductor doping type
Semiconductor doping characteristic: Only *uniform* doping is available at this time
Gate electrode: Gate electrode type. Options are: aluminum, poly-silicon, tungsten, or any specific material (for which, one needs to specify the work-function from below)
Gate workfunction: Specify workfunction for any arbitrary gate contact material.

3.1.2. *Parameter:*

Fixed charge density in gate insulator: Fixed bulk charge density divided by q (that is number density) in gate insulator
Interface trap charge density in gate insulator: Interface trap charge density divided by q in gate insulator

3.1.3. *Environment:*

Ambient temperature: Temperature around the device in K (range: 77 - 500)
Initial voltage: Initial value for the voltage sweep in V (range: -20 - 20)
Final voltage: Final value for the voltage sweep in V (range: -20 - 20)
Number of voltage steps: Integer number (range: 1 - 200)
High frequency value for AC Analysis: For C-V Characteristics (order of 10^6), in Hz (value > 1 Hz)
Low frequency value for AC Analysis: For C-V Characteristics (order of 10 Hz), in Hz (value > 0.01 Hz)
Minority carrier lifetime for electrons in ns: Smaller value gives better low-

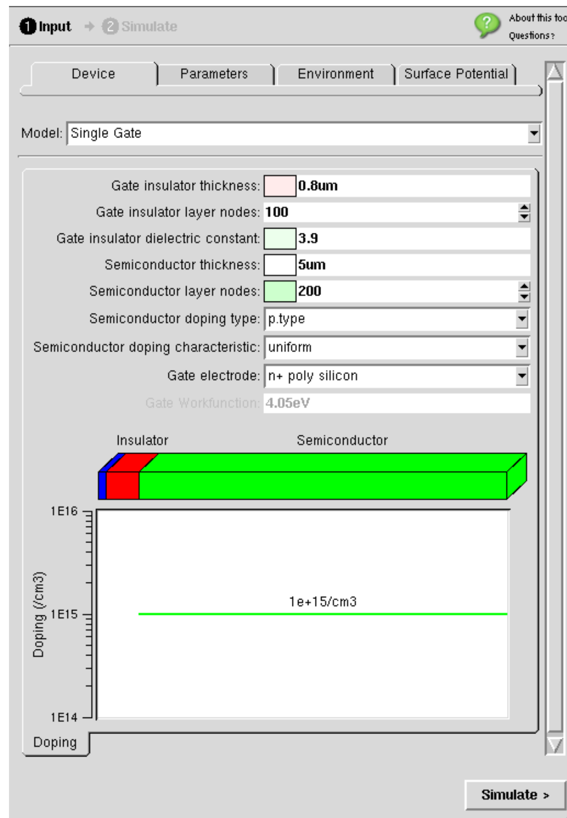


Fig. 5. Input deck: *Device*.

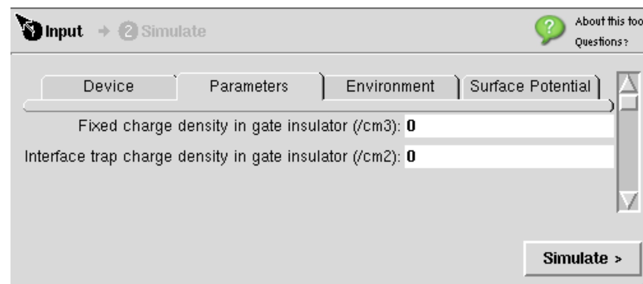


Fig. 6. Input deck: *Parameters*.

frequency CV curve.
Minority carrier lifetime for holes in ns: Smaller value gives better low-frequency CV curve.

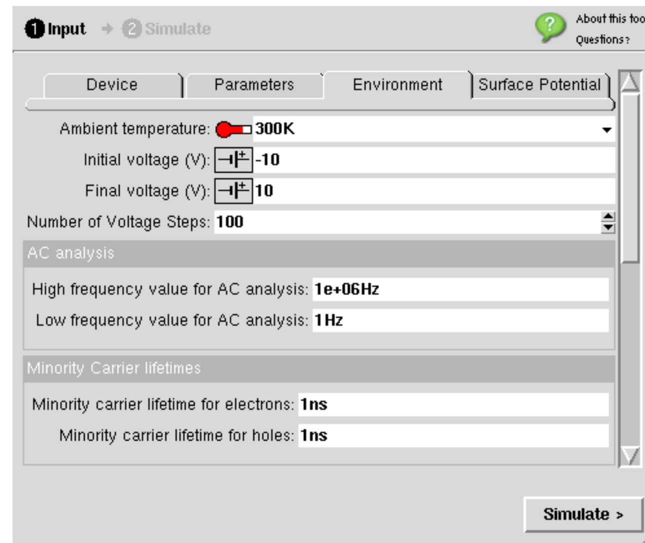


Fig. 7. Input deck: *Environment.*

3.1.4. *Surface Potential:*

Check the box to plot surface potential. Note that this is a standalone section in the simulator and uses the analytical models to compute surface potential as a function of applied gate voltage (which we have already covered in Section 2).
Temperature: Temperature around the device in K (range: 4 - 500)
Acceptor dopant density: For a p-type substrate, in $/cm^3$(range: 0 $/cm^3$ – $10^{22}/cm^3$)
Donor dopant density: For a n-type substrate, in $/cm^3$ (range: 0 $/cm^3$ – $10^{22}/cm^3$)
Intrinsic carrier density: in $/cm^3$ (range: 0 $/cm^3$ – $10^{22}/cm^3$)
Oxide thickness: in μm (range: 0 - 10)
Gate voltage range minimum, V_g min: in V (range: -20 - 20)
Gate voltage range maximum, V_g max: in V (range: -20 - 20)
** In double gate device, input deck provides multiple options for left gate

and right gate options for all gate related parameters.

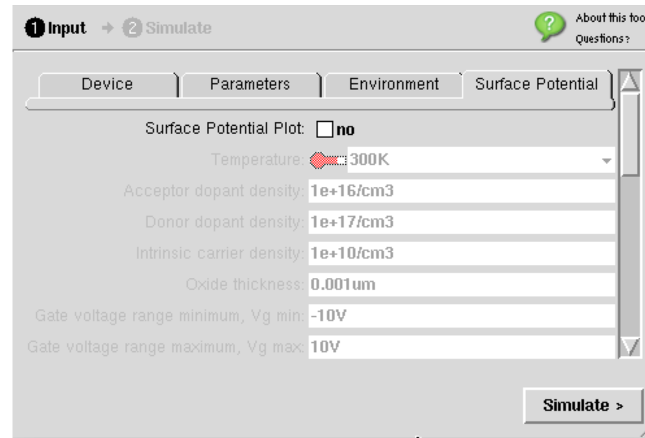


Fig. 8. Input deck: *Surface Potential*.

3.2. *Output Analysis*

Below is a list of of technologically important parameters, values of which can be extracted from the CV characteristic of a MOS structure.

3.2.1. *Extraction of device parameters from CV measurements*

(1) Capacitance:
An equivalent circuit model for capacitances of an MOS structure is shown in (Fig. 9). Here, capacitance depends on the frequency of applied signal (Fig. 10). At high frequency, electron concentration remains fixed at an average value and electron layer does not respond to V_g. So, the channel capacitance, $C_{ch} = 0$ and the semiconductor capacitance depends on the capacitance of the depletion region only ($C < Cox$).

For low frequency, electrons can be generated by thermal excitation fast enough to be in phase with the applied signal and can respond to V_g. Since channel is very thin ($t_{ch} \approx 0$), channel capacitance, $C_{ch} \approx \frac{\varepsilon}{t_{ch}} \approx \infty$. Hence, capacitance of substrate and channel in parallel becomes infinity, ($C_s + C_{ch} = \infty$).

The net capacitance leads to

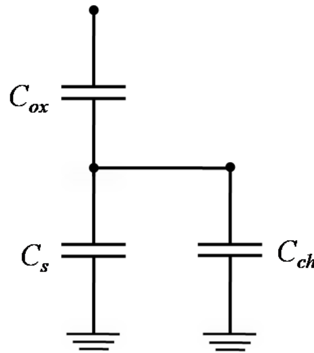


Fig. 9. Equivalent circuit for MOS capacitances.

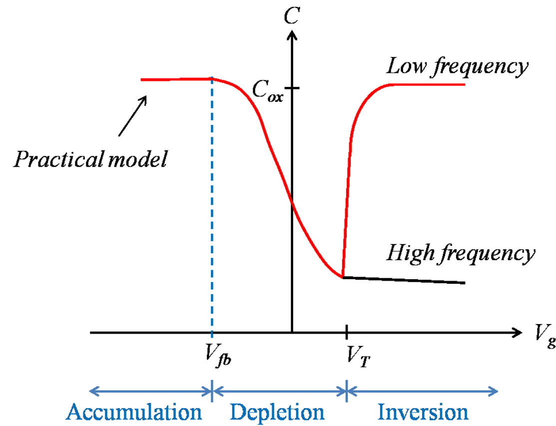


Fig. 10. Typical CV characteristic for a p-substrate MOS capacitor.

$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s+C_{ch}} = \frac{1}{C_{ox}} + 0 = \frac{1}{C_{ox}}$.
So, the capacitance tends to go back to the Cox level ($C \approx C_{ox}$).
In the following, we will use the low-frequency CV characteristic to define and extract some other parameters.

(2) Oxide thickness:
Calculating oxide thickness is fairly simple and is given by,

$$T_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{C_{ox}} \quad (3)$$

Where,

T_{ox} is the oxide thickness (cm),
C_{ox} is the oxide capacitance (Farad, F),
ϵ_o is the free space permittivity and
ϵ_{ox} is the permittivity of oxide (F/cm).

(3) Flatband capacitance:
To have capacitance, we need applied voltage and charges available to respond to the voltage. At zero temperature ($T = 0K$), there are no charges to respond, so we do not have any capacitance. But at room temperature ($T = 300K$), we have intrinsic charges in the device and thermal potential ($V_0 = \frac{kT}{q}$). At $V_g = 0$, as there would not be any depletion layer, ideally all capacitance for flat-band (C_{fb}) should come from oxide capacitance (C_{ox}). But in reality, we see a slight drop in the capacitance because of debye length due to thermal potential.

$$L_D \sim \sqrt{\frac{2\varepsilon_{si}kT}{q^2 N_A}} \tag{4}$$

Where,
L_D is the Debye length (cm),
ϵ_{si} is the permittivity of silicon (F/cm),
kT is the thermal energy at room temperature, $(300K)(4.046\times10^{-21}J)$,
q is the electron charge ($1.60219 \times 1019C$),
N_A is the acceptor doping density (cm^{-3}).
So, at $V_g = 0$, the flatband semiconductor capacitance is, $C_{s,fb} = \frac{\varepsilon_0\varepsilon_s}{L_D}$.
So, the flatband capacitance of the device is,

$$C_{fb} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{s,fb}}} \tag{5}$$

(4) Threshold voltage:
In the CV curve, the threshold voltage is the point where surface potential (ϕ_s) is twice the Fermi potential (ϕ_F). This point in the curve corresponds to strong inversion. The threshold voltage is calculated as follows:

$$V_T = V_{fb} + 2\phi_F + \frac{\sqrt{4qN_A\varepsilon_{si}\phi_F}}{C_{ox}} \tag{6}$$

Where,
V_T is the threshold voltage (V),
ϕ_F is the Fermi potential (V),

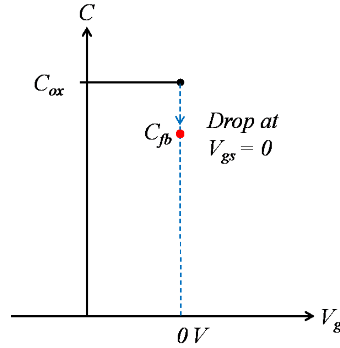


Fig. 11. Effect of thermal potential (and Debye length) on MOS flat-band capacitance.

$$\phi_s = 2\phi_F = 2\frac{kT}{q}ln\frac{N_A}{n_i} \tag{7}$$

and V_{fb} is the flatband voltage (V).
In a practical MOS Capacitor, poly-silicon is used instead of metal as gate contact. Therefore, due to the variation in work function at the gate/oxide interface, MOSCap operation deviates from the ideal case. Also, work function of semiconductor ϕ_s varies as a function of doping density. The metal-semiconductor work function difference is given by $(\Phi_{ms} = \Phi_m - \Phi_s)$. As a result of this, the flat-band potential becomes, $V_{fb} = \Phi_{ms} - \frac{Q_i}{C_{ox}}$, where Q_i is the interface charge.

(5) Substrate doping concentration:
Doping concentration of the semiconductor sustrate can be extracted from the slope of the CV characteristic, which at the depletion-layer edge is given by[1]

$$N_a(W) = \frac{2}{q\epsilon_{si}\frac{d(\frac{1}{C^2})}{dV}} \tag{8}$$

3.2.2. *Sample Simulations*

During the course of building our first device, we will learn how to use the MOSCap tool and plot and extract the output quantities conveniently.

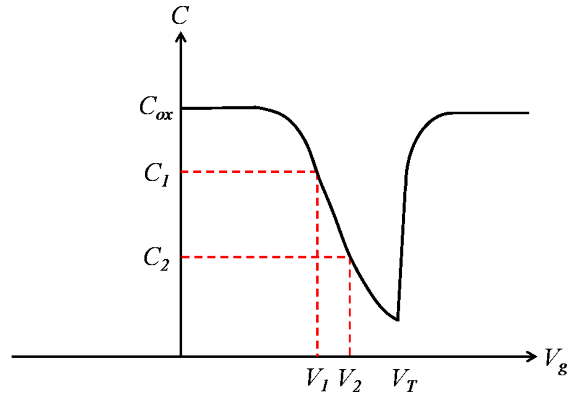


Fig. 12. Substrate density can be extracted from the slope of the CV characteristic.

Device Description: Design and simulate a single-gate MOS Capacitor with the following specification.
Structural Specifications
Substrate: p-Type
Substrate Thickness: 5 μm
Substrate Doping Density: 1e+15 $/cm^3$; Uniform
Gate material: n-type poly-silicon
Insulator: SiO2; Thickness = 0.8 μm; Dielectric Constant, $\epsilon_{ox} = 3.9$
External Environment:
Temperature: 300 K
Initial Voltage: -10 V
Final Voltage: 10 V
Low frequency value: 1 Hz
The rest, for the time being, we can keep what we get as default in the tool. Snapshots of the Input Decks/Phases for this simulation are shown in Figs. 5 - 8:

Outputs: A typical Output Deck is shown in Fig. 13. All of the plots that available from this simulator are, as of now, one-dimensional. Access to *simulation parameters* used is available from the bottom panel/tab on the deck.

A range of outputs are available in the drop-down menu shown in Fig. 14. The user can download and save the outputs (as *data* or *image*) by clicking the download button available at the top right corner (Fig. 15). Different

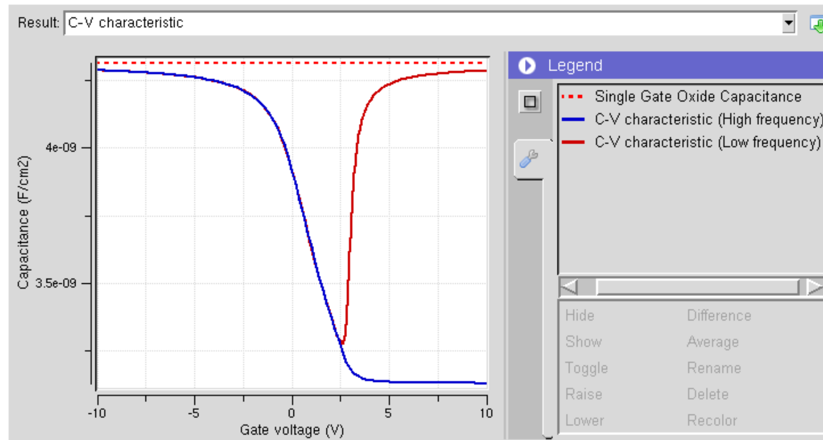


Fig. 13. The output deck.

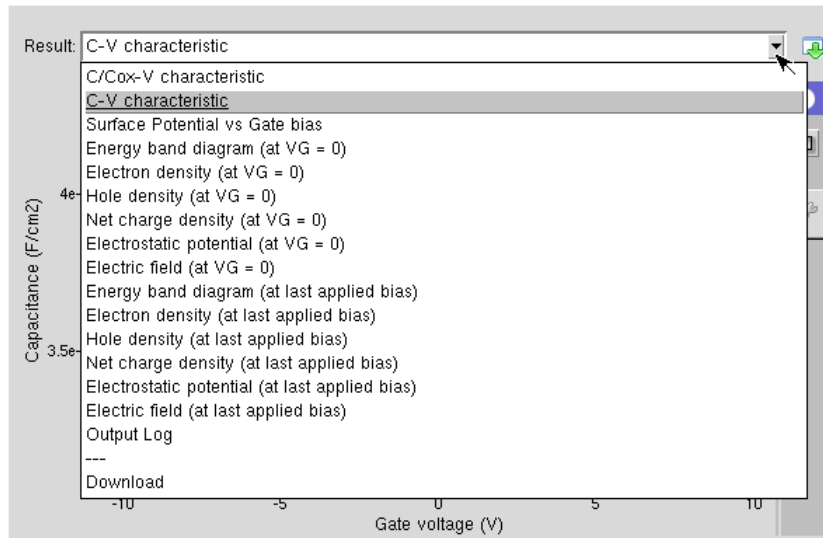


Fig. 14. Output drop down menu.

formatting options are also available for the image Type, Axis, Legend, and Layout (Fig. 16).

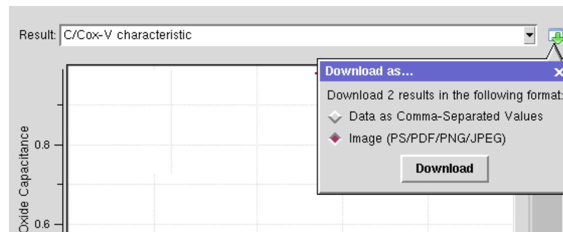


Fig. 15. Download *data* or *image*

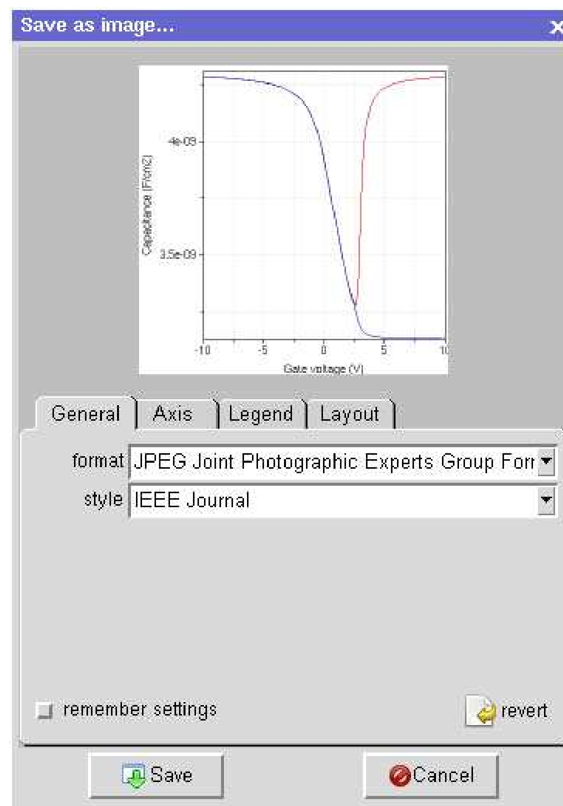


Fig. 16. Downloading and saving options.

Description and Analysis of Outputs:

(1) CV Characteristic: The CV characteristics of the MOS structure show

both the normalized (by C_{ox}) and net capacitance as a function of the gate voltage. This is probably the most important curve the user would look for. As explained in an earlier Section, several different parameters can be *extracted* from the CV characteristic. Please note that the simulator does not, by default, calculate and provide these values.

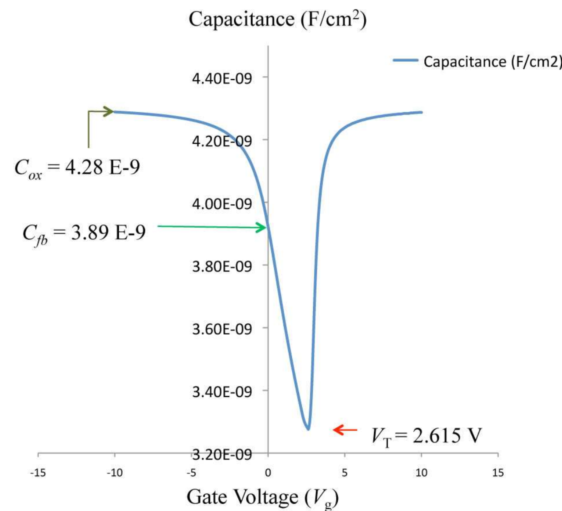
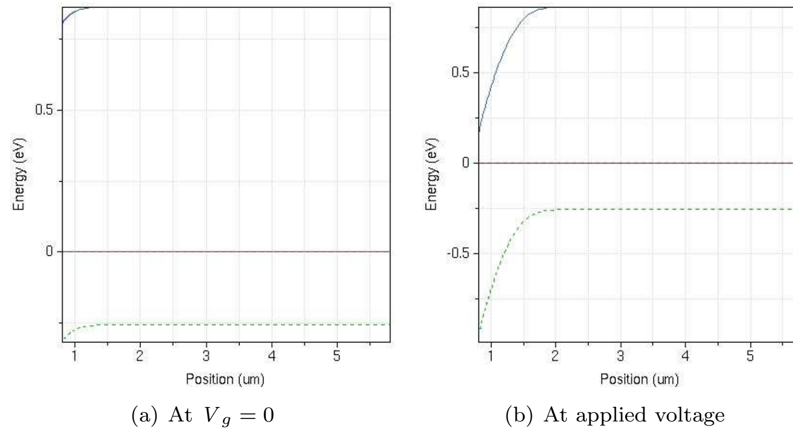


Fig. 17. CV Characteristic of the MOS structure.

(2) Energy Band Diagram: Conduction band, Valence Band, and the Fermi level are available for equilibrium ($V_g = 0$) and biased (for last applied bias) conditions.

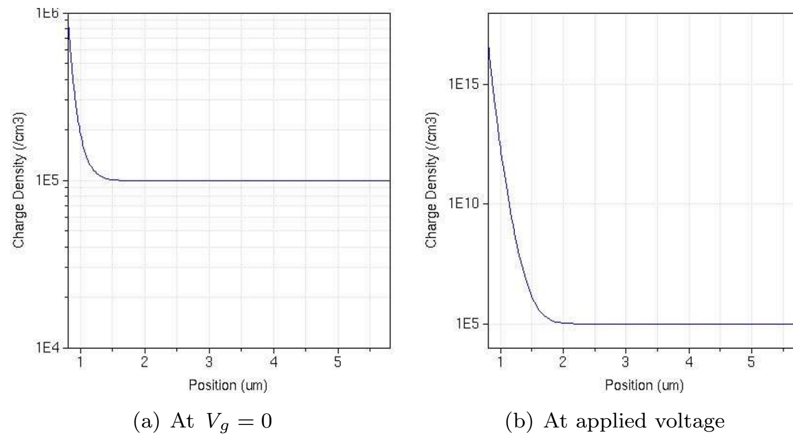
In Fig. 18(a), because of the work function difference, a small band bending is observed at the oxide/semiconductor interface even when the device is unbiased. As expected, in the biased case (Fig. 18(b)), the band bending is steeper which leads to the creation/induction of the channel region populated by minority electrons.

(3) Electron Density: Electron density plots in the semiconductor substrate are available for equilibrium ($V_g = 0$) and biased (last bias point) conditions (Fig. 19(a) and Fig. 19(b)).



(a) At $V_g = 0$ (b) At applied voltage

Fig. 18. Potential energy vs. Distance along the substrate depth.

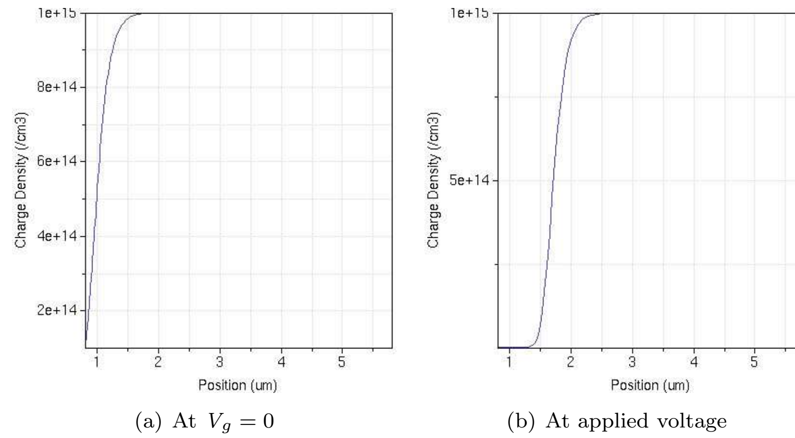


(a) At $V_g = 0$ (b) At applied voltage

Fig. 19. Electron Density vs. Distance along the substrate depth.

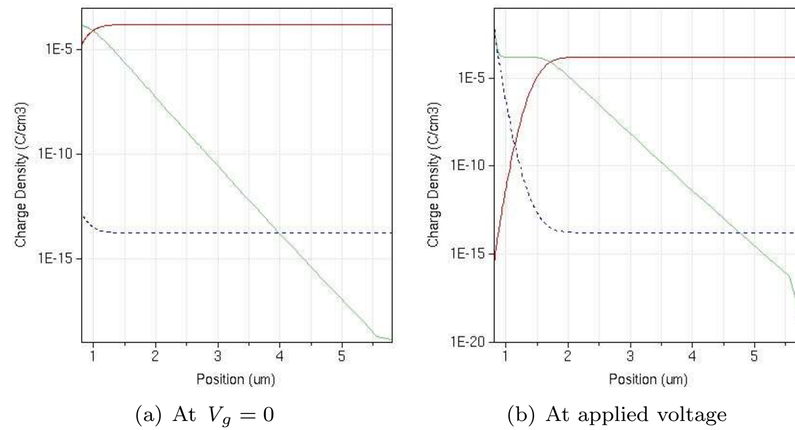
(4) Hole Density: As electron density, hole density plots in the semiconductor substrate are also available for equilibrium ($V_g = 0$) and biased (last bias point) conditions (Fig. 20(a) and Fig. 20(b)). However, the hole density plots depict an oppositive trend as a function of the gate voltgae.

(5) Net Charge Density: Net charge density is defined as $\rho = q(N_A - N_D + n - p)$ and shown in Fig. 21(a) and Fig. 21(b).



(a) At $V_g = 0$ (b) At applied voltage

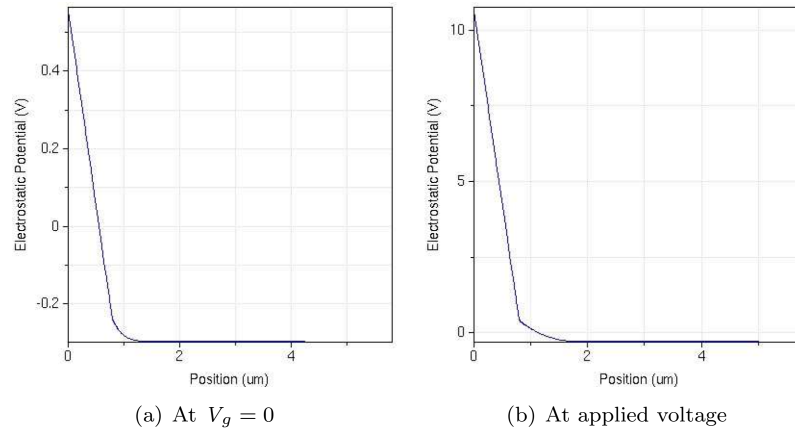
Fig. 20. Hole Density vs. Distance along the substrate depth.



(a) At $V_g = 0$ (b) At applied voltage

Fig. 21. Net charge density vs. Distance along the substrate depth.

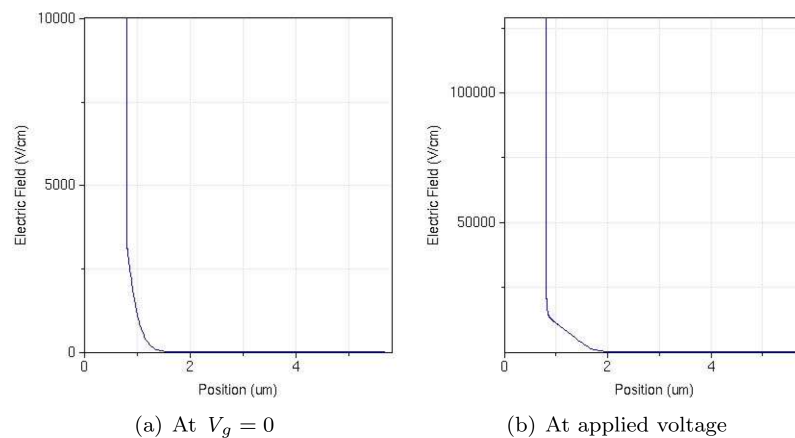
(6) Electrostatic Potential: The potential is defined as $V = const - q \times E_c$ and hence has an opposite trend with regard to the band diagram. The equilibrium potential distribution (Fig. 22(a)) originates from the gate/semiconductor workfunction difference. Fig. 22(b) shows the same at biased condition. Also, due to absence of charges, potential varies *linearly* with distance in the oxide region.



(a) At $V_g = 0$ (b) At applied voltage

Fig. 22. Electrostatic potential vs. Distance along the substrate depth.

(7) Electric Field: Electric field is defined as $\xi = -\nabla V$ and shown in Fig. 23(a) and Fig. 23(b) for equilibrium and biased conditions. Noticeable is the sharp transition of the electric field at the oxide/semiconductor interface, which arises from the discontinuity (inhomogeniety) of the dielectric constants (3.9 for oxide and 11.7 for silicon) therein.



(a) At $V_g = 0$ (b) At applied voltage

Fig. 23. Electric field intensity vs. Distance along the substrate depth.

Comparison of Outputs: Simulation tools on nanoHUB.org, in general, allow users to run multiple sets of simulations (by varying one or a group of parameters) and compare the results on a single plot. To illustrate this, here, simulaiton results are presented and compared for two different values for the substrate doping concentration of a MOS capacitor (Fig. 24). As expected, by comparing the two CV curves, the user can immediately see that the use of a higher substrate doping density leads to an increased threshold voltage.

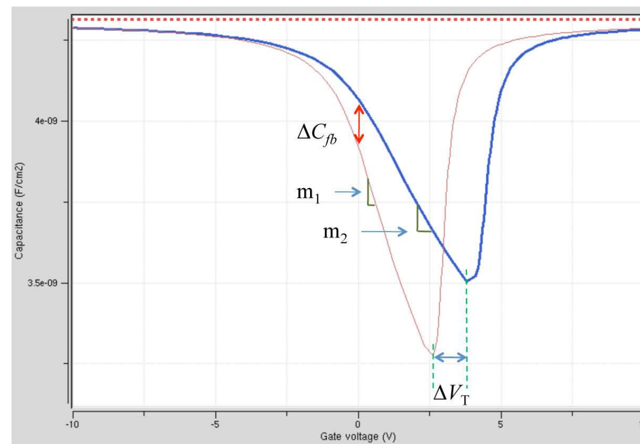


Fig. 24. CV characteristics of two MOS samples for $N_{A1} = 10^{15}\,cm^{-3}$ and $N_{A2} = 2 \times 10^{15}\,cm^{-3}$

4. Conclusion

The MOSCap tool on nanoHUB.org numerically describes the CV characteristics of single-gate and dual-gate silicon MOS structures. The user can extract an array of important device parameters from the CV characteristic (such as threshold voltage, semiconductor doping density, typr of gate contact, gate insulator thickness), which not only provide a better understanding of the underlying physics, but help design improved MOSFETs using such MOS building blocks. MOSCap is based on the Padre simulation tool developed by Mark Pinto, R. Kent Smith, and Ashraful Alam at Bell Labs. The tool has three noteworthy limitations: 1) There is no models available for the study of quantum mechanical effects; 2) Users

are not allowed to perform the AC analysis for a range of frequencies; and 3) MOSCap does not have sequence plots, that is, users cannot see what happens in the intermediate steps between $V_g = 0$ and the last applied bias. The MOSCap tool was published on nanoHUB on April 06, 2006. As of November 16, 2012, the tool has served 3,296 users worldwide, who have run a total of 32,189 simulation runs.

References

1. Y. Taur and T. H. Ning *Fundamentals of Modern VLSI Devices* 2009: Cambridge University Press.